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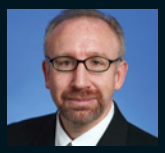
JUNE 9
Issue 11/2011
www.edn.com



PEERING INSIDE A PORTABLE, $200 CANCER DETECTOR

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DESIGNING IR GESTURE-SENSING SYSTEMS

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EDA TOOLS PAVE PATH TO 3-D ICs

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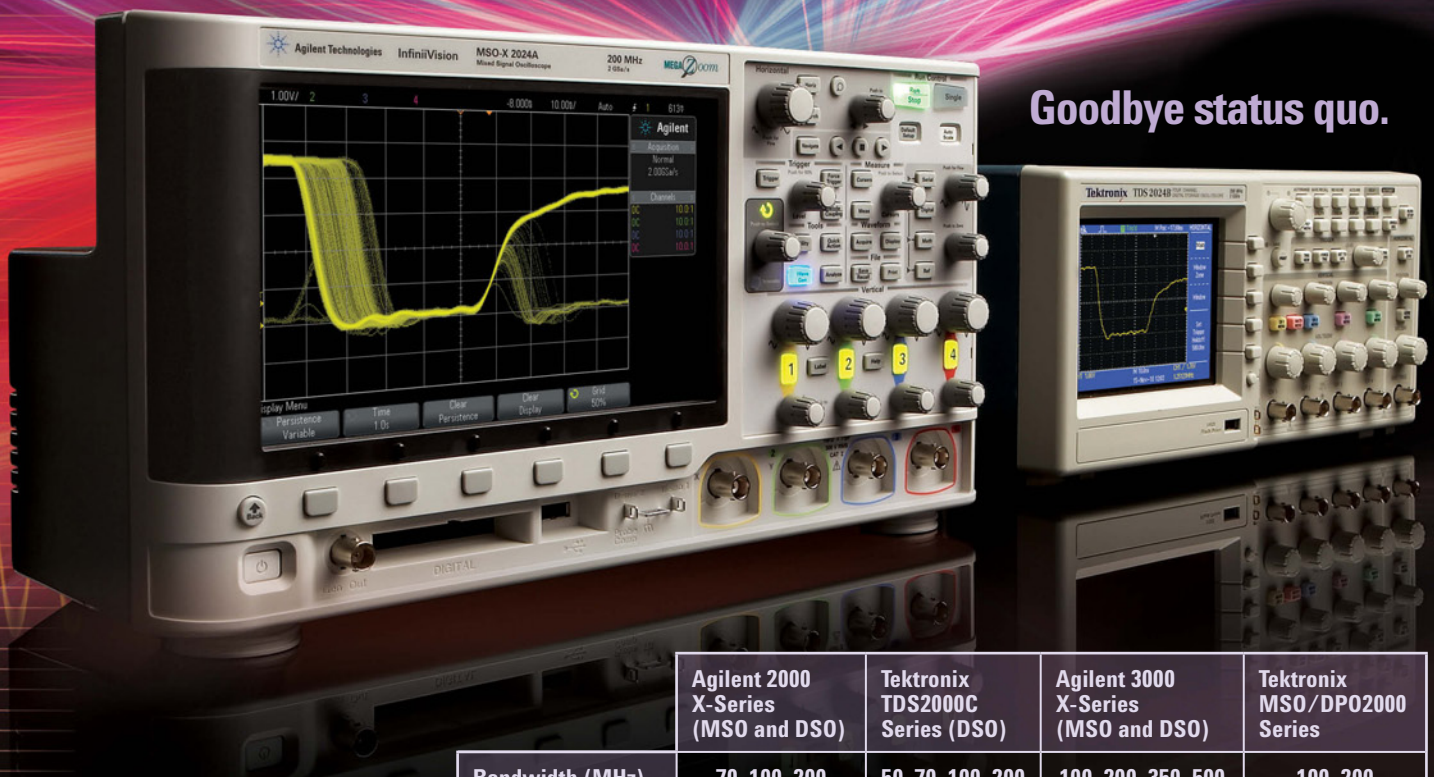
Hello future.



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Max memory depth	100 kpts	2.5 kpts	4 Mpts	1 Mpt
Max update rate (waveforms/sec)	50,000	200**	1,000,000	5,000
Fully upgradable	Yes	No	Yes	No
Function Generator	Yes	No	Yes	No
Notes:	**Refer to Agilent Pub 5989-7885EN for update rate measurements Data for competitive oscilloscopes from Tektronix publications 3GW-25645-0 and 3GW-22048-1 Measurements taken on same signal using Agilent MSOX2024A and Tektronix TDS2024B Screen images are actual screen captures and scopes are shown to scale			

*All prices are in USD and subject to change

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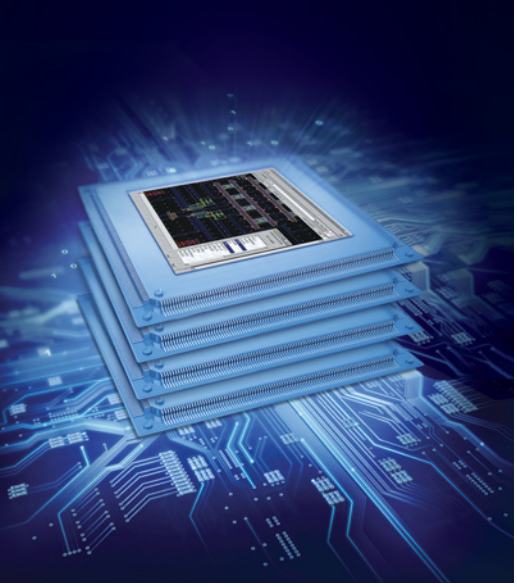

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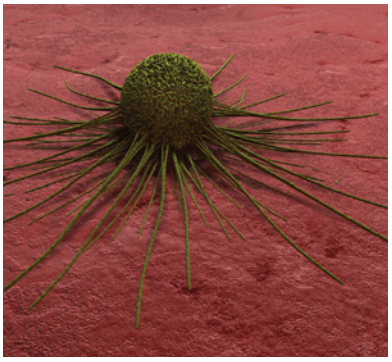
EDA tools pave the way to 3-D ICs

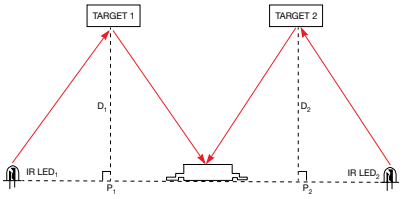
by Mike Demler, Technical Editor



Peering inside a portable, $200 cancer detector

by Jim MacArthur, Electronic Instrument Design Laboratory, Harvard University

pulse

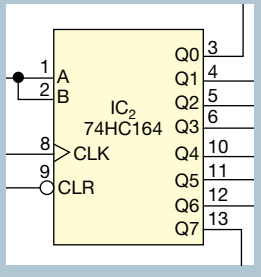


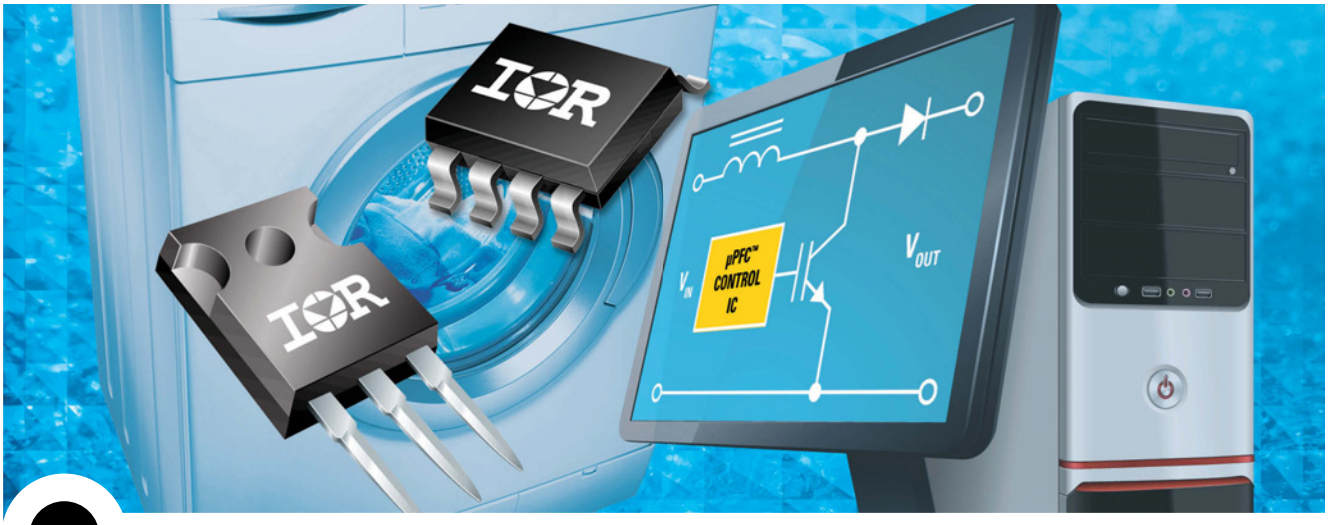
Designing IR gesture-sensing systems

by Alan Sy, Silicon Laboratories

COVER: ISTOCK

DESIGNIDEAS





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IRG4(B/IB)C20W	Discrete	6.5	2.6	TO-220AB; TO-220 FullPak
IRG4(B/IB/P)C30W		12	2.7	TO-220AB; TO-220 FullPak; TO-247AC
IRG4(B/P)C40W		20	2.5	TO-262; TO-220AB; TO-247AC
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PRYING EYES

In *EDN*'s Prying Eyes, we peer inside an end-user consumer gadget, a reference design, or any other interesting electronics-enabled thing we can get a good look at. Prying Eyes aims to illuminate the tough design decisions the engineers responsible for the design had to make. Find the entire Prying Eyes archive at www.edn.com/pryingeyes, or sample a couple of installments at the links below:

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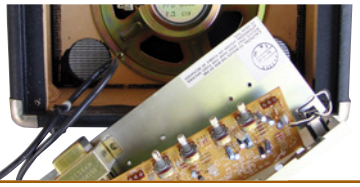

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Volume 56, Number 11 (Printed in USA).

BY BRIAN DIPERT, SENIOR TECHNICAL EDITOR

What happens when software undermines hardware's potential?

In a recent article, I mentioned the RIM (Research in Motion) PlayBook (see "ARM versus Intel: a successful stratagem for RISC or grist for CISC's tricks?" *EDN*, April 7, 2011, pg 24, http://bit.ly/hQwGEu). I showcased it as one of the first announced design wins for Texas Instruments' OMAP (Open Multimedia Applications Platform) 4 SOC (system on chip). I also am well-acquainted with Motorola's Xoom tablet, which the company based on Nvidia's Tegra 2 dual-core SOC. Both the PlayBook and the Xoom have impressive hardware potential, but the currently available operating systems and application suites for both platforms sabotage that potential.

I have long felt that the PlayBook's dearth of support for native e-mail, calendaring, contacts, and similar applications—except through a Web-browser interface if the service provider offers that option—would constrain the device to being little more than a Palm Foleo-like device, dependent on a tethered handset. Don't forget that the Palm Foleo flopped.

RIM's primary market focus continues to be enterprises, in which the company's handsets are well-entrenched. Yet, RIM is also aggressively targeting consumers with its first tablet. The PlayBook's home-screen icons for Gmail, Facebook, and Twitter are currently nonfunctional placeholders. And those consumers who are AT&T subscribers, even if they have BlackBerry mobile phones, are completely out of luck: The cellular carrier's distaste for unsanctioned tethering has compelled it to reject the BlackBerry Bridge app, thereby blocking the tablet's access to a handset's e-mail, calendar, and contacts data.

Now consider the Xoom. Unlike its Android 2.x-based handset and tablet peers, the Android 3.x-based Xoom doesn't yet allow use of the microSD (secure-digital) slot for optional application installations, for file transfers, or even for users' data storage. The Motorola tablet's shortcomings extend beyond software to hardware. Although the company plans 4G (fourth-generation) LTE (long-term-evolution) cellular-data support, it is still shipping devices with 3G (third-generation)-only transceivers. And, although the 4G upgrade will be free to Xoom owners, it will require that users do without the device for several days to several weeks while it undergoes upgrading at a Verizon or a Motorola service center.

Tablets aren't the only devices whose makers have neutered their features. For example, the Nintendo 3DS Web browser is not yet functional. These situations are especially baffling; it's one thing to omit a feature, but shipping a system with icons for—or other active references to—nonfunctional apps is especially insensitive to consumers. These systems' designers were perhaps uncomfortable with the decision to go to production with half-baked products, but upper management's desires to establish a market presence overrode the designers' concerns. In the case of the two tablets, company officials were attempting to slow the momentum of the Apple iPad. With the Nintendo 3DS, the twin motivations were to compete against smartphones and bolster a sagging corporate bottom line.

It's difficult to construct a case that early-production decisions for any of these devices were good ones. Early-adopter buzz—either positive or negative—is a powerful phenomenon, and recovering from initial negative press, assuming that recovery is possible, requires substantially more time, money, and effort than does launching a more solid product in the first place.

The ship-it-early strategy sometimes pans out. Consider that the Xbox 360 hit the market a year before the Sony PlayStation 3 did, and, despite the Microsoft console's well-documented thermal issues, it flip-flopped the respective companies' market positions with the earlier-generation Xbox and PS2.

More often than not, though, a premature launch ends up playing out poorly for the supplier—and the ecosystem. Releasing software updates every two weeks, as RIM reportedly plans to do, is admittedly better than nothing at all, but it's not as good as waiting a few months and providing a more robust feature foundation. It also subjects customers to periodic update hassles that they shouldn't have to bother with.

Upper management's desires to establish a market presence overrode the designers' concerns.

Updatable, nonvolatile code-storage devices, such as hard-disk drives and flash memory, enable upgradable software, which in turn fuels the temptation to launch early. The problem seems to have recently become worse, and I'm not sure what manufacturers can do to dodge the obstacles they keep hitting. What do you think? EDN

+ Read an expanded version of this column in the Brian's Brain blog at www.edn.com/110609eda.

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EDITED BY FRAN GRANVILLE

pulse

INNOVATIONS & INNOVATORS

Easy-to-use benchtop source/measure units provide wide voltage-versus-current ranges

Agilent Technologies has announced the B2900A series, its first line of compact benchtop SMUs (source/measure units) for testing semiconductors, components, and materials. The units provide fast, simple current-versus-voltage characterization of semiconductors; active and passive components; and materials in research, development, manufacturing, and education. For example, the voltage range is ±210V, and current ranges are ±3A dc and ±10.5A pulsed. Sourcing is precise, and measurements are accurate with minimum resolution of 100 nV and 10 fA.

The intuitive GUI (graphical user interface) includes a 4.3-in. color LCD that supports graphical and numerical displays in single, dual, graph, and roll modes. By easing the quick completion of a variety of measurements and providing the ability to view the results on a color display, the B2900A series performs interactive testing, debugging, and characterization faster than do conventional SMUs.

In automated testing, the B2900A series units archive data at a maximum swept-operation reading rate from the sourced or measured quantity to the IEEE-488 bus of 12,500 readings/sec—twice the rate of competing SMUs. Under program control, the new SMUs support the SCPI (standard commands for programmable instruments) command set, providing Basic compatibility and enabling easy migration from conventional SMUs.

The B2900A series comprises the one-channel B2901A and B2911A and the two-channel B2902A and B2912A models. The B2901A and B2902A have current resolution of 100 fA; the B2911A and B2912A have current resolution of 10 fA. Capabilities such as the number of displayed digits, measurement resolution, minimum timing interval, and supported view modes further distinguish the instruments, making it easy to select a combination of price and performance that fits your testing needs.

It can be confusing to use conventional stand-alone instruments, such as voltage/current sources and meters, switches, and arbitrary-waveform generators, to perform current/voltage measurements. An SMU integrates these capabilities in one compact instrument.

Many Agilent SMUs, including the B2900A series, can operate as four-quadrant voltage/current sources, electrical loads, voltage/current meters, pulse generators, and arbitrary-waveform generators. These capabilities enable the instruments to perform a variety of dc and low-frequency ac measurements without changing connections or using additional equipment. US list prices begin at $5671.

—by Dan Strassberg

▷**Agilent Technologies**, www.agilent.com/find/B2900A.

TALKBACK

"I wouldn't be too quick about blaming gear heads; a lot of really weak EEs out there simply do not understand the fundamentals of solder joints. And EEs do know everything."

—*EDN* reader "Andy T," in *EDN*'s Talkback section, at http://bit.ly/kXfx5u. Add your comments.

Although small, the B2912A performs a variety of benchtop current/voltage-testing functions that would otherwise require many instruments and much greater setup time and cost.

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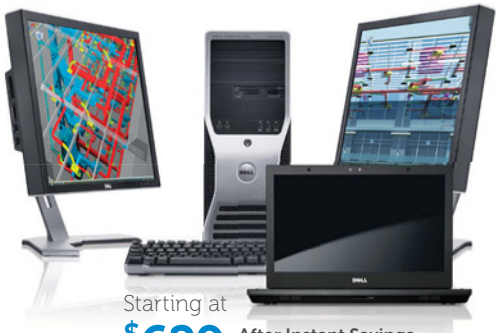

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MIT uses virus to increase solar-cell efficiency

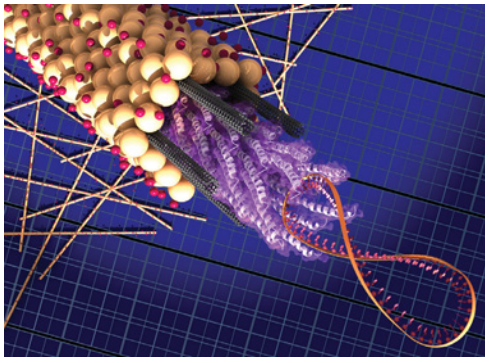
Researchers at the Massachusetts Institute of Technology claim to have increased the power-conversion efficiency of solar cells by nearly one-third through the use of tiny viruses to perform detailed assembly work at the microscopic level (**Reference 1**). The MIT researchers based their findings on the fact that carbon nanotubes can enhance the efficiency of electron collection from a solar cell's surface. They used a genetically engineered version of the M13 virus, which normally infects bacteria, to control the arrangement of the nanotubes on a surface. This approach keeps the tubes separate so that they can't short out the circuits and keeps the tubes apart so that they don't clump—two problems that have plagued previous attempts to use carbon nanotubes in solar cells.

The system the researchers tested uses lightweight and inexpensive dye-sensitized solar cells, whose active layer comprises TiO_2 (titanium dioxide), rather than the silicon that conventional solar cells use. The same techniques can be applied to quantum-dot and organic solar cells. In tests, adding the virus-built structures enhanced the power-conversion efficiency to 10.6% from 8%, almost a one-third improvement.

The researchers achieved this efficiency improvement even though the viruses and the nanotubes make up only 0.1% of the weight of the finished cell. "A little biology goes a long way," says Angela Belcher, a WM Keck professor of energy who worked on the project. The researchers believe that they can even further ramp up the efficiency with additional work.

The M13 virus comprises a strand of DNA (deoxyribonucleic acid) attached to a bundle of peptides, which attach to the carbon nanotubes and hold them in place. A coating of TiO_2 attaches to dye molecules, surrounding the bundle. The viruses improve one step in the process of converting sunlight to electricity: funneling electrons toward a collector, from which they can form a current that flows to charge a battery or power a device. Adding the carbon nanotubes to the cell provides a more direct path to the current collector, according to Belcher.

The viruses possess peptides—short proteins that can bind tightly to the carbon nanotubes, holding them in place and separating them from each other. Each virus can hold five to 10 nanotubes; about 300 of the virus' peptide molecules hold each of these nanotubes firmly in place. The researchers engineered the virus to produce a coating of TiO_2, a key ingredient for dye-sensitized solar cells, over each of the nanotubes. That step put the TiO_2 in close proximity to the wirelike nanotubes that carry the electrons. The same virus performs the two functions in succession; the virus switches from one function to the next by changing the acidity of its environment. This switching feature is an important new capability that this research demonstrates for the first time. The viruses also make the nanotubes soluble in water, which makes it possible to incorporate the nanotubes in the solar cell using a water-based process that works at room temperature.



The M13 virus comprises a strand of DNA (the figure-8 coil on the right) attached to a bundle of peptides (the corkscrew shapes in the center), which attach to the carbon nanotubes (gray cylinders) and hold them in place. A coating of titanium dioxide (yellow spheres) attaches to dye molecules (pink spheres), surrounding the bundle. More of the viruses with their coatings appear in the background (courtesy Matt Klug, Biomolecular Materials Group, MIT).

Japan, South Korea, and Taiwan have already commercialized dye-sensitized solar cells. Solar experts believe that the industry will adopt such processes if the addition of carbon nanotubes can improve their efficiency through the virus process. Because the process would just add one step to a standard solar-cell manufacturing process, it should be easy to adapt production facilities and should be possible to implement relatively rapidly. Italian company Eni funded the research through MIT's Solar Futures Program.

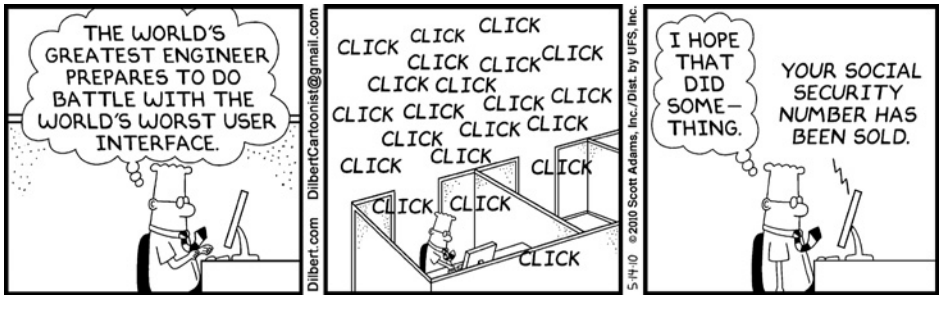
—by Suzanne Deffree

▷**Massachusetts Institute of Technology**, www.mit.edu.

REFERENCE

1 Dang, Xiangnan; Hyunjung Yi; Moon-Ho Ham; Jifa Qi; Dong Soo Yun; Rebecca Ladewski; Michael S Strano; Paula T Hammond; and Angela M Belcher, "Virus-templated self-assembled single-walled carbon nanotubes for highly efficient electron collection in photovoltaic devices," *Nature Nanotechnology*, April 24, 2011, http://bit.ly/lJysWi.

DILBERT By Scott Adams

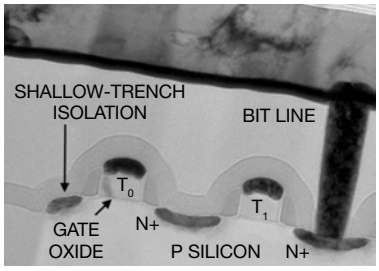


New technology goes beyond OTP

Silicon-IP (intellectual-property) vendor Kilopass Technology has added multitime programmability to antifuse-based nonvolatile memory. An antifuse-based memory can be programmed by breaking down a silicon-oxide barrier to set the state of the memory bit in a two-transistor cell. Like a ROM, programming with antifuse memory has traditionally been an OTP (one-time-programmable) process. With the announcement of Itera technology, Kilopass adds multitime programmability of as many as 1024 cycles for memories with as much as 1 Mbit of storage capacity. The company targets applications in software protocol stacks for wireless applications in Wi-Fi and Bluetooth, low-frequency data logging, and SOCs (systems on chips) that require periodic software updates.

Antifuse memory is smaller and offers less programmability than flash memory, but the Kilopass technology allows you to manufacture in a standard CMOS-logic process and scale it to 28 nm and smaller processes without any additional process steps. The result is lower manufacturing cost for trimming analog blocks, storing small amounts of code, and verifying security identification. Access time is 20 nsec in the 40-nm version of Itera. For larger capacity requirements, the Kilopass Gusto memory IP, which the company introduced in 2010, offers as much as 4 Mbits of nonvolatile OTP memory.

Kilopass offers Itera with a per-design license fee for the use of Itera or as a per-wafer royalty. Designers can then use Itera for applications with requirements of 32 bits to 1 Mbit. It is available now for manufacturing at foundries, including TSMC (Taiwan Semiconductor Manufacturing Co, www.tsmc.com), GlobalFoundries (www.globalfoundries.com), and UMC (United Microelectronics Corp, www.umc.com), in 40-nm bulk silicon. Kilopass also plans to make Itera available in 65- and 55-nm processes this year.



The Kilopass memory IP provides one-time or multitime programmability with a two-transistor antifuse cell for manufacturing nonvolatile memory in standard CMOS-logic processes.

—by Mike Demler

▷**Kilopass Technology**, www.kilopass.com.

KaiSemi claims automatic FPGA-to-ASIC conversion

06.09.11

Using a variety of processes from 90 to 500 nm, fabless semiconductor vendor KaiSemi Ltd recently unveiled automated conversion, a process to convert most current FPGA designs to drop-in ASIC replacements. According to Tomer Kabakov, the company's vice president of marketing, the flow begins with a design review. The customer provides a frozen FPGA netlist and an SDF (standard-delay-format) file; functional test vectors; pin definitions, including electrical requirements; and a checklist of additional information, such as timing constraints, clock frequencies, and test strategy. Kabakov notes that strong indicators of the convertibility of a netlist are the successful operation of the design in production and the completeness of the test-vector set. Beyond that, the review looks for known conversion obstacles, such as asynchronous blocks or multigigabit I/Os.

KaiSemi then runs its conversion tool. A run takes 12 to 24 hours, depending on the original design's size. The tool transforms the FPGA netlist into a cell-based ASIC netlist using a proprietary set of libraries that KaiSemi developed for the purpose. This process is not a simple mapping of look-up tables, multiplexers, and registers into cells, Kabakov says. The tool infers logic functions from the FPGA netlist and attempts to map them into functional blocks from the libraries. KaiSemi also attempts to map third-party IP (intellectual-property) blocks directly rather than through netlist conversion.

The approach should not only produce better results for a random-logic netlist but also address two problems in conversion: block RAM and DSP blocks. The tool examines the configuration of block RAM and its wrapper in the FPGA netlist, infers the actual RAM function the design uses—a small multiport, say, or a large FIFO (first-in/first-out) buffer with overflow and underflow flags—and instantiates the correct function in the ASIC netlist. It does not attempt to replicate the block RAM itself.

Similarly, the tool examines the netlist's use of FPGA DSP blocks and infers an optimized datapath. The cell-based netlist in KaiSemi's older processes can usually keep up with the maximum clock rate the customer is applying to the nominally faster DSP block in the FPGA.

The flow moves from translation to formal and functional netlist verification and from there to a conventional ASIC back-end flow: scan/test insertion, resimulation, and physical design. By translating netlists rather than resynthesizing RTL (register-transfer-level) logic, KaiSemi stays closer to the original design and substantially shortens the front-end-design time. By inferring intent from the netlist, however, the tool escapes slavishly duplicating the FPGA-specific fine structure of look-up tables, registers, and hard-function blocks.

KaiSemi charges no NRE (nonrecurring-engineering) costs for the conversion service. The vendor calculates the unit price for the resulting ASIC based on the complexity of the design, the manufacturing cost, and the amortization of the cost conversion.—by Ron Wilson

▶**KaiSemi**, www.kaisemi.com.

VOICES

NXP's Rick Clemmer: bright lights, big opportunity

Rick Clemmer, executive director, president, and chief executive officer of NXP Semiconductors, recently talked with *EDN*, discussing speculation on NXP's future, reviewing the company's most recent quarter and capacity shifts, and revealing how NXP's NFC (near-field-communication) strategy is allowing the company to shine with major lighting-application moves, including its GreenChip smart-lighting product, which NXP calls an "Internet address for every light bulb," and its intent to make its JenNet-IP (Internet Protocol) ultra-low-power, IEEE 802.15.4-based wireless-connectivity network-layer software available under an open-source license. The following is an excerpt of that interview. You can read the full interview at www.edn.com/110609pa.

NXP's first-quarter product revenue from continuing operations of $979 million was up 4.4% sequentially, and net profit was $187 million. How did you accomplish this growth?

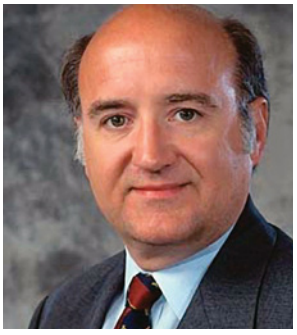
A Some of the things that contributed to that [growth] were that, for our ID [identification] business, which has been capacity-limited, we were able to pull forward some of the increased manufacturing capacity we were bringing online. It allowed us to really drive increased growth. We had set expectations to be roughly flat, and we were able to achieve a 4.4% sequential growth. Most of our peer group was negative in that quarter because of its inherent cyclic [nature].

How is NXP's cost-savings effort, the Redesign Program, going?

A We're most of the way through the Redesign Program. We've said that we will achieve $900 million to $950 million in savings. Through the end of last quarter, we were at [approximately] $811 million or so. We have $100 million plus to go, but we are basically on track. It's just about executing that [goal]. There's not a lot of additional increase to come.

NXP's recently announced GreenChip smart lighting screams "Internet of Things." What's your take on the phenomenon, and how does the Internet-address-for-every-light-bulb initiative fit in?

A When [Google Executive Chairman] Eric Schmidt talked about Web 2.0, he talked about NFC and the convenience it would bring to users. Clearly, the technology we provide [will] facilitate that [convenience] and … make [it] work for Google and for everyone else. The [GreenChip smart-lighting action] takes us away from the Internet of people to the Internet of Things—the ability to control things, whether it's lighting, home appliances, white goods, or



security cameras. It's the ability to have that control and have a significant impact on energy consumption. [Approximately] 25% of home-energy consumption is in the form of lighting, and at least 30% of that energy consumption is wasted because it is in the form of heat as opposed to lighting itself. By us providing this capability, it allows someone to address that [consumption] so that they can have significant energy savings.

We are also announcing the opening of our software stacks, similar to what we did with NFC. Applications associated with NFC [are] limited only by the imagination of the application developers. Opening the software stacks on the "smarter home" gives us the ability to drive those same kinds of inherent accelerations on energy-cost savings. We think there is a clear opportunity for governments to participate in this [technology], but, even without their participation, the deployment costs associated with [this move for users] can be paid back in roughly a half-year. It offers the opportunity to significantly reduce overall energy consumption; it's in line with what governments have prioritized for reducing carbon-dioxide emissions and energy requirements. And we think that the ability to facilitate and drive that [idea] with strong partnerships with GreenWave and TCP allows us to establish the proof in our ability to drive what we think is a unique and exciting technology.

Will lighting be as big a market for NXP as NFC is?

A When we look at the total market, it's different. I think it can be bigger than NFC, potentially. When we look at the combination of what we've called the smart connected network, which includes the automation of white goods and e-metering as well as lighting automation, we think that the market for semiconductors can be about $4.5 billion by 2015, and roughly a fourth to a third of that [amount] will be associated with lighting and lighting automation. So there's a significant amount that will take place even without [lighting].

There's a lot going on with NFC. ZTE, for one, is using NXP's NFC. Visa last month unveiled its entry into "digital wallets." And Apple and Google have stated interest. How's the competitive outlook from your standpoint?

A A lot of people are starting to talk about it. We've said that, when 30 or 40% of handsets have NFC in them, then it will be integrated into the connectivity chip. We fully expect at some point that the radio portion itself will get integrated. We are trying to ensure that we are focused on the total solution and that the total solution includes a combination of the secure element, the radio, as well as the software. When the radio gets integrated, we want to be sure that we are providing the secure element for hundreds of millions of units associated with it. **—interview conducted and edited by Suzanne Deffree**

AT THE FRONTIERS OF SIMULATION

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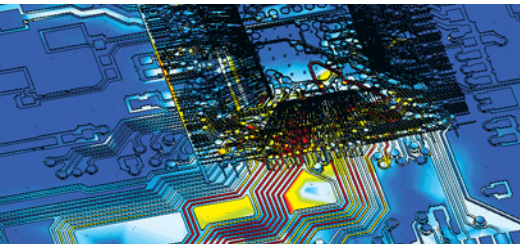

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CHANGING THE STANDARDS

BY PALLAB CHATTERJEE, CONTRIBUTING TECHNICAL EDITOR

Energy-efficient electronics

You can optimize many aspects of nanoelectronics and MEMS (microelectromechanical-system) technology. The University of California—Berkeley has an ongoing research program that focuses on creating approaches to making energy-efficient circuits and devices. The program covers materials, magnetics, photonics, MEMS devices, circuit designs, and modeling.

Researchers in the photonics realm are working on developing smaller vertical- and lateral-facing LED-laser sources for short-range interconnect. One of the goals of developing these high-speed circuits is to as quickly as possible transfer information to the adjacent chips. However, sending the information in a traditional electrical current or voltage fashion generates and wastes heat. Further, physical-process variation affects resistance and capacitance for minimum delay. The new devices are targeting LED photonics, including light sources, light-steering methods, and detectors. The research is on the fundamental level from materials and process-flow technologies. These new devices are targeting a tenfold improvement over current energy levels as their operating goal.

Similarly, researchers are considering new device architectures. For example, one of the researchers, Tsu-Jae King Liu, PhD, has been looking at MEMS that manufacturers can make reliably using standard processing and that can find use in new applications at a lower power. One of the greatest sources of power and current loss is leakage in the off state of a transistor acting as a switch. Liu and her team have been working on circuits based on electrostatic MEMS devices that have 0A off-state current. **Figure 1** shows the cross sections for the off and on states of a four-transistor relay circuit. This device has a physical air gap between the two states; as a result, the device has high off-state resistance. When the device makes a connection, it has a relatively low on-resistance.

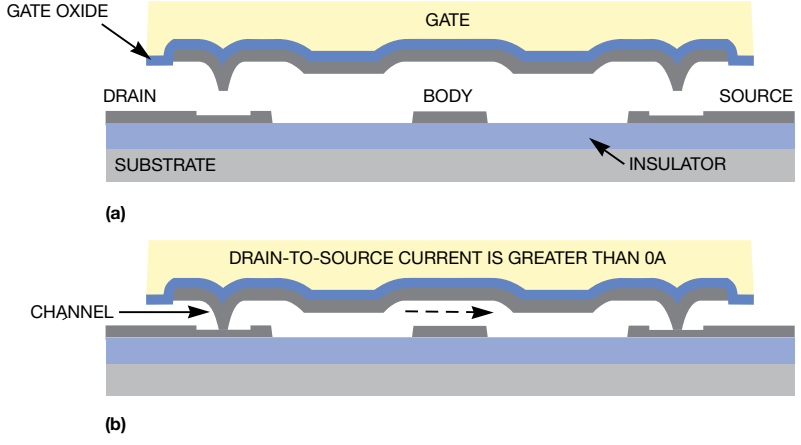

Figure 1 The cross sections for the off state (a) and on state (b) of a four-transistor relay circuit have a physical air gap between the two states; as a result, the device has high off-state resistance (courtesy University of California—Berkeley).

This sort of device is useful for both logic functions with ultralow-steady-state power draw and for switched-power-rail applications on standard nanoelectronics circuits. The researchers created the devices using atomic-layer deposition and tested them in the lab. The devices exhibit a 100-nsec switching time for a less-than-2V gate-switch control voltage. The devices show no detectable wear even after the preliminary testing of 1 billion on/off cycles.

Eli Yablonovitch, PhD, heads the program. Yablonovitch also heads a basic materials program. His team is researching some magnetic and electromagnetic materials with a combination of elements. The team is reviewing these materials both for their standard memory capacities for nonvolatile and 3-D stacked-memory elements and for active devices. The researchers are targeting these materials for the practical realization of those technologies and others. Researchers are also studying the materials to see whether they can improve traditional rotating storage media, such as disk drives.

On the active-response side, researchers are using these materials for near-0V power logic that can also support circuitry to help sense, amplify, and distribute the data in the devices. The use of these materials is for direct applicability on traditional CMOS processes, on the silicon-interposer technology for 3-D stacked devices, and as stand-alone MEMS-wafer processes.

All of these technologies will drive change for the industry and its quest for a more-than-tenfold reduction in power in the next five years. EDN

Pallab Chatterjee is on the IEEE Nanotechnology Council.

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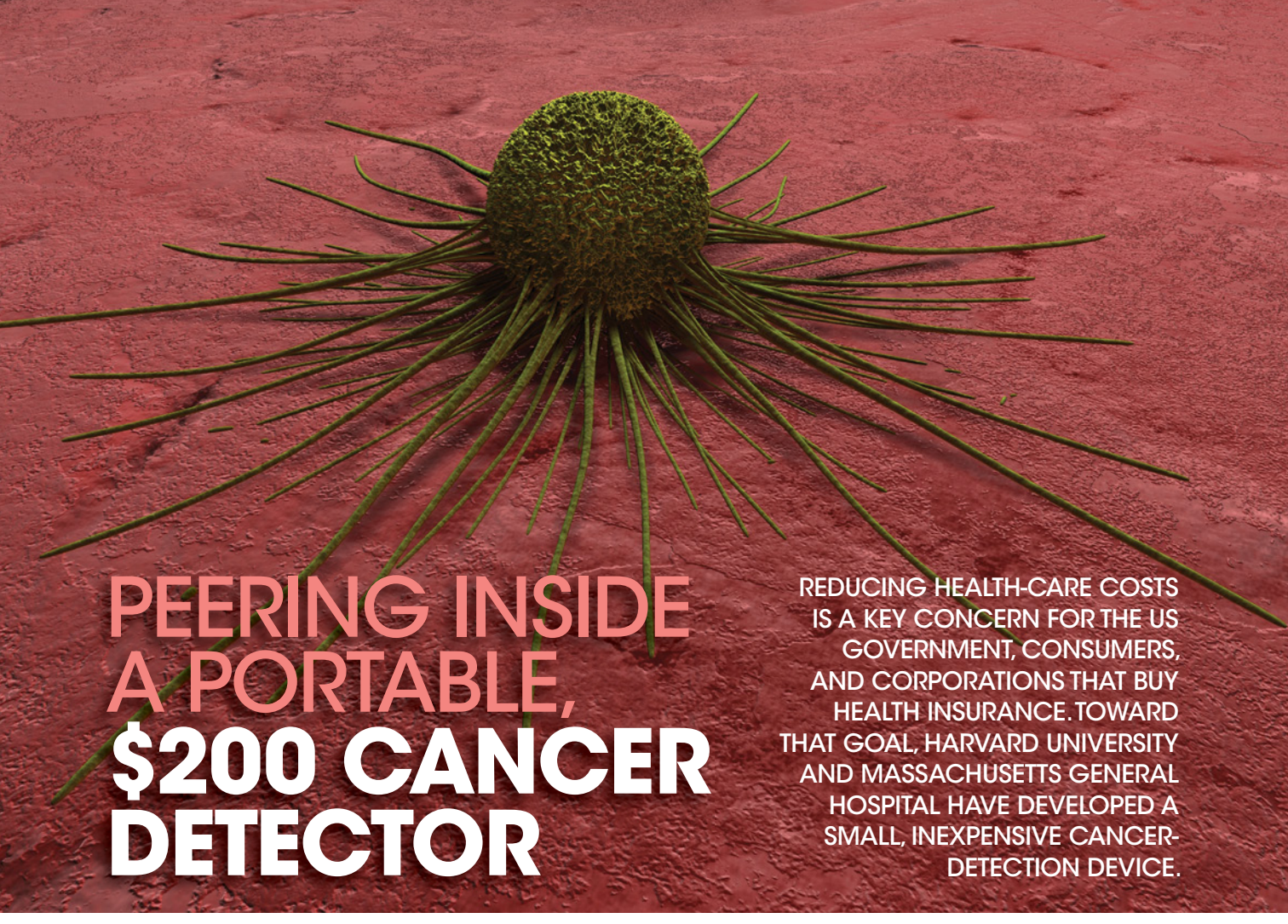

PEERING INSIDE A PORTABLE, $200 CANCER DETECTOR

REDUCING HEALTH-CARE COSTS IS A KEY CONCERN FOR THE US GOVERNMENT, CONSUMERS, AND CORPORATIONS THAT BUY HEALTH INSURANCE. TOWARD THAT GOAL, HARVARD UNIVERSITY AND MASSACHUSETTS GENERAL HOSPITAL HAVE DEVELOPED A SMALL, INEXPENSIVE CANCER-DETECTION DEVICE.

BY JIM MACARTHUR • ELECTRONIC INSTRUMENT DESIGN LABORATORY, HARVARD UNIVERSITY

As part of a project to design the electronics for a portable, low-cost cancer detector, I had to understand NMR (nuclear magnetic resonance), a measurement technique that excites and measures the spin precessions of atomic nuclei. I also relied on the expertise of Hakho Lee, PhD, and David Issadore, PhD, two researchers at Massachusetts General Hospital's Center for Systems Biology. Lee had been using magnetic-relaxation switching to explore ways to reduce the size and bulk of an NMR machine to the point at which it could be carried into the field to perform medical diagnostics.

Lee had refined an NMR-based technique for detecting tuberculosis-specific proteins, using a fist-sized permanent magnet and a rack full of electronics. My task was to squeeze that rack into a book-sized unit. The electronics box needed to create a string of RF pulses of precisely controlled frequency in the range of 20 to 30 MHz, and the phase between the first and subsequent pulses also had to change by a precisely controlled amount. This discussion requires some background on NMR techniques.

NMR 101

"NMR" refers to any of several measurement techniques that excite and measure the spin precessions of atomic nuclei. Think of a proton as a sphere with its charge uniformly distributed throughout. The proton's spin can be understood as making it rotate at a fixed rate. This rotation makes every bit of charge move in a circle. Then, analogous to current in a solenoid, these moving charges create a magnetic field, or "moment," that aligns on the spin axis. As with a macroscopic magnet, this magnetic moment tends to align with an externally applied magnetic field.

Just as perturbing a gyroscope makes it precess around the axis of the external gravitational field, perturbing a proton with a burst of RF (radio-frequency) energy at a certain frequency in the presence of a magnetic field makes its moment precess at the same frequency. This resonant frequency, the Larmor frequency, is a function of the magnetic-field strength in the proton's neighborhood. Irish physicist and mathematician Joseph Larmor in 1896 proposed the Larmor frequency, which stipulates

IMAGE: THINKSTOCK

that a magnetic moment in a magnetic field tends to align with that field. As the proton's magnetic moment gradually realigns with the external magnetic field, the proton emits RF energy, again at its Larmor frequency.

Not only protons but also many atomic nuclei—those possessing an odd number of protons or neutrons—have spin, with different Larmor frequencies. Hydrogen's frequency, for example, is 42.58 MHz/tesla. One tesla equals 10,000 gauss; one gauss is approximately equal to the earth's magnetic-field strength. Nitrogen's frequency is 3.09 MHz/tesla. Conversely, the common isotopes of oxygen and carbon have no net spin; therefore, NMR cannot detect them.

In NMR spectroscopy, each element has a unique frequency, and nearby atoms slightly shift a given atom's Larmor frequency, making it possible to infer the molecular structure of a sample (**Reference 1**). NMR spectroscopy's success depends on correctly interpreting tiny changes in Larmor frequencies, which themselves are functions of the surrounding magnetic field. As such, the technique requires care in creating a uniform and stable magnetic field.

In addition to determining a proton's Larmor frequency, the RF signal also provides the two time constants of the decay in spin precession. After a proton is perturbed, it relaxes to bulk thermal equilibrium with a time constant of T_1. Interaction with neighboring spins causes a shorter time constant, T_2. These interactions detune the individual precessions, causing destructive interference and shortening the decay time.

T_2 describes the immediate magnetic environment of each nucleus and, thus, its molecular composition; T_2 also provides information about the inhomogeneity of the bulk magnetic field. The greater the inhomogeneity, the more the individual Larmor frequencies will interfere and the faster the RF signal will decay. In all but the most carefully controlled magnetic fields, the bulk field's inhomogeneity effects completely overwhelm the more interesting information about a proton's immediate neighborhood. You can solve this problem using spin echo, an elegant technique, which works as follows.

Start by sending an RF pulse with enough energy to bring the precession angle of the magnetic moments down to 90° with respect to the bulk magnetic field. At first, the precessions are all in phase with each other, with emitted RF at a maximum. Nearly immediately, however, the Larmor frequencies cause the precessions to dephase. After a few milliseconds, the dephasing reaches its maximum, and the net radiated RF is consequently low.

Next, send another RF pulse that is twice as long as the original. Because

AT A GLANCE

- Each element has a unique Larmor frequency, and nearby atoms slightly shift a given atom's frequency. The combination of these two actions makes it possible to infer the molecular structure of a sample using NMR (nuclear-magnetic-resonance) spectroscopy.
- Include no more than one new concept per subsystem because fixing two bugs is an order of magnitude harder than fixing one.
- Maintaining documentation discipline is difficult when you are trying to meet deadlines; design reuse without a document trail, on the other hand, is practically impossible.
- A digital camera with a macro lens is a useful tool for documenting hardware changes.
- The biggest barrier to using an FPGA approach may be software. If some new IP (intellectual-property) core doesn't work as its manufacturer advertised or some new software revision makes your board stop working, you are at the mercy of technical support.

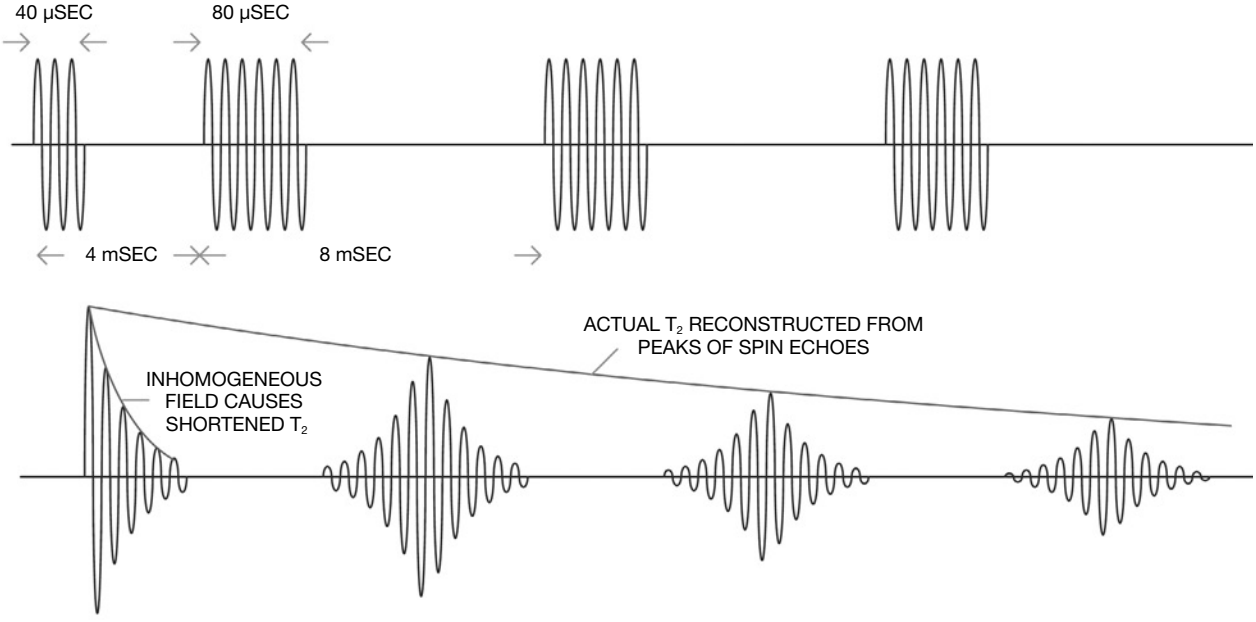

Figure 1 By plotting the decay of the peaks of the echoes, you can get an accurate assessment of T_2. Times are approximate and adjustable.

the first pulse rotates each magnetic moment by 90°, the second pulse rotates it 180° more. To picture what happens next, imagine holding a closed paper fan before your face and then slowly opening it to represent the dephasing process. The righthand part of the fan represents the faster moments, and the lefthand part represents the slower moments. Now, flip the fan around. The faster moments are now on the left; they begin catching up with the slower moments, closing up the fan and restoring the RF signal.

You can repeat this process until the precessions completely decay (**Figure 1**). By plotting the decay of the peaks of the echoes, you can get an accurate assessment of T_2.

This article provides only a cursory treatment of NMR, using classic analogies to describe an inherently quantum effect. However, my goal was to provide a taste of the engineering issues. Most of the Larmor frequencies of interest are in the decade between 10 and 100 MHz, which, from an engineering standpoint, is a good place to be because lots of earlier RF-design concepts are applicable. Although the design of the receiver chain isn't trivial, for example, it's a piece of cake compared with tuning in and identifying short-wave radio signals from thousands of miles away.

The SNR (signal-to-noise ratio) increases with the static magnetic field, so keep the field as high as possible. For large samples, this means using a massive magnet with supercooled coils. For small samples, on the other hand, you can create fields larger than 1 tesla with a handheld permanent magnet. The small magnet in the DMR-3, the official name for this instrument, creates a roughly 0.5-tesla field (**Figure 2**). Relaxation times are on the order of a few milliseconds to a few seconds. Demodulated signals range to tens of kilohertz; you must acquire data at 100 kHz, for example, for a second or so. This is not, in other words, a taxing data-acquisition problem.

IDENTIFYING THE PROBLEM

While I was working on this project, Lee and Issadore were working on their goal of making the NMR portable. In pursuit of this goal, Lee used magnetic-relaxation switching, which binds magnetic nanoparticles to proteins by first binding the nanoparticles to protein-specific antibodies, which in turn bind to proteins. Once these nanoparticles find the target proteins, they clump together, significantly decreasing the spin-relaxation time of nearby atoms. In other words, clumped nanoparticles translate to a shorter T_2.

My design needed to demodulate the returned signal at the RF frequency and then digitize it at 100,000 samples/sec for several seconds. Several stacked runs' results would be transmitted to a host computer for analysis. All pulse timing needed to be accurate to 1 µsec or better. The host computer controls all parameters over USB (Universal Serial Bus)- and asynchronous-interface ports. The box had to be rugged and portable, and

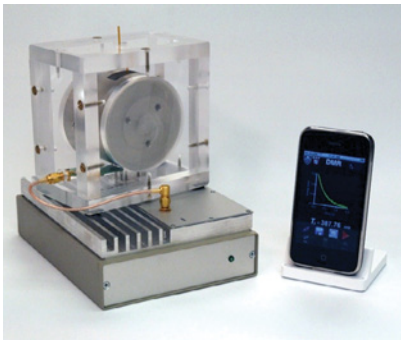

Figure 2 The DMR-3 uses a smartphone as a display.

the first deployment would be in Africa (**references 2** and **3**) in three months.

DESIGNING THE SYSTEM

The package for the system is a Lansing Instrument MicroPak enclosure. The top cover is replaced by a custom-milled piece of aluminum, doing double duty as a heat sink for the RF transmitter and a quiet enclosure for the RF-receiver chain. The instrument contains four PCBs (**Figure 3**). The controller, ADC, and DDS (direct-digital-synthesizer) boards live in the bottom section, and the new board containing the RF-receiver signal chain is up top (**Figure 4**). The controller board includes a Texas Instruments TMS320F28235 Delfino DSC (digital-signal controller), an ISSI (Integrated Silicon Solution Inc) IS61WV102416 asynchronous 1M-word×16-bit SRAM, and an FTDI (Future Technology Devices International) FT245 USB-interface chip.

The Delfino DSC performs speedy, 32-bit math and I/O operations, and it comes with an array of peripherals perfect for instrumentation, including high-resolution PWMs (pulse-width modulators) and time stampers, UARTs (universal asynchronous receivers/transmitters), CAN (controller-area-network) circuitry, and DMA (direct-memory-access) controllers. Most important, it features full silicon support for runtime debugging—not just for setting breakpoints but also for viewing, altering, and logging memory and register space when the processor is running at full speed.

I considered using an FPGA but decided against it. Although the cost of materials doesn't strongly drive my design decisions, I can't justify replacing a $25 microcontroller with a $250 FPGA. And the BGA packaging typical of FPGAs is an issue for small production runs. The biggest barrier to using an FPGA approach, however, is software. Every FPGA developer I know has a horror story of some new IP (intellectual-property) core that didn't work as advertised or how some new software revision made a board stop working.

That said, I *do* scatter small FPGAs and CPLDs (complex programmable-logic devices) throughout my designs as insurance against mistakes and to allow for reuse in unanticipated ways; the DMR-3 contains two of them, for example. As a side benefit, programmable logic can often unscramble buses and do other board-cleanup chores, turning a risky six-layer PCB design into a simpler four-layer configuration. The Delfino DSC talks to the DDS board via a clocked serial protocol implemented with GPIO (general-purpose input/output) pins. The DDS board contains a pair of synchronized Analog Devices AD9954 DDS chips, which generate RF signals at the same frequency, but with programmable phase separation. One DDS chip generates the NMR transmitted signal; the other creates the local oscillator that mixes the received signal to baseband.

The AD9954 is admittedly something of an odd choice. Alternatively, I could have used a dual-DDS AD9958 chip, which I already had because I'd used it for a physics experiment that required eight phase-staggered sine waves slowly swept from 10 kHz to 20 MHz. This problem is a nasty one in the analog domain, but it's not so bad with a bunch of DDS chips. From them, a pair of now-obsolete AD8326 CATV (cable-television) amplifiers amplify the RF signals, illustrating the point that baseband amplifiers, which get faster every year, can process RF signals in the 10- to 100-MHz range. A search on the Web for "CATV" and "DSL" (digital-subscriber-line) produces lots of useful amplifiers that work into the tens of megahertz.

From the DDS board, the NMR's transmitter and local-oscillator signals transfer through the aluminum top block and into the RF cavity, containing the only new board in the system. For this design, I stayed with the receiver-signal chain that Lee had tested: a pair

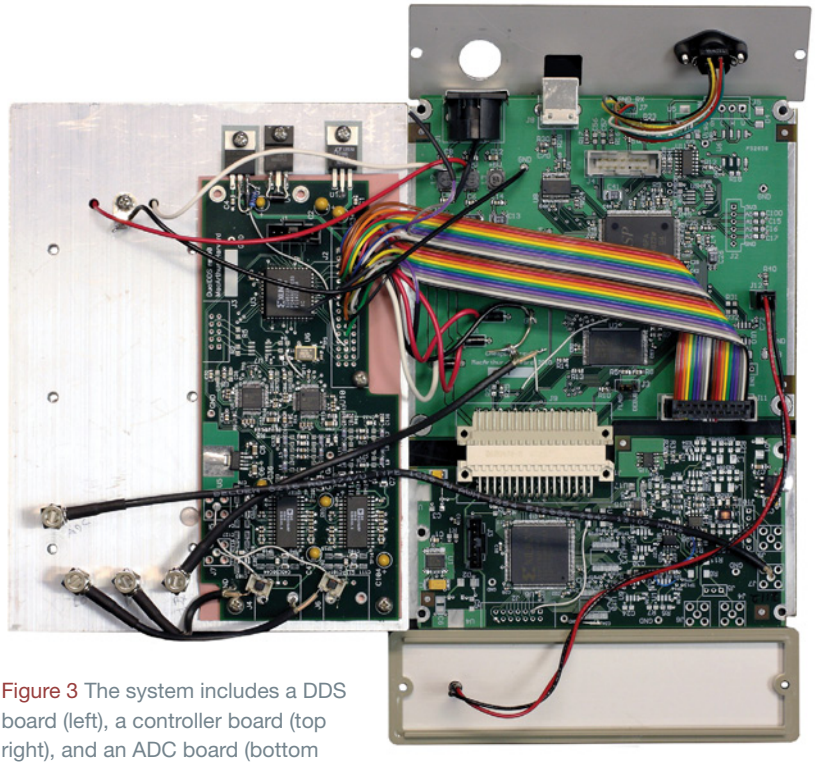

Figure 3 The system includes a DDS board (left), a controller board (top right), and an ADC board (bottom right). Because the DDS and power-amplifier chips get hot and because supplemental ventilation is impossible, the DDS board mounts on the top-cover heat sink with Bergquist foam.

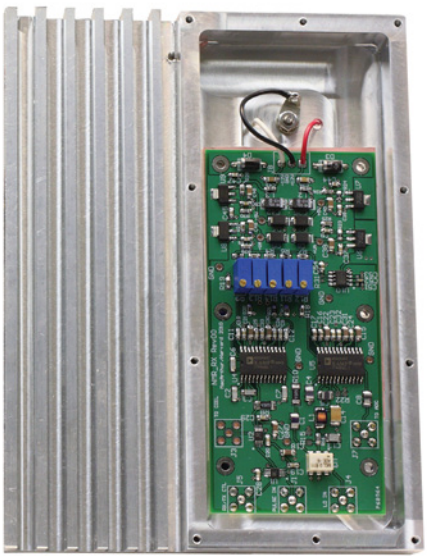

Figure 4 In the RF section of the design, the trimming potentiometers control the gains of the AD604 amplifiers.

of dual variable-gain AD604 amplifier chips, with a Mini-Circuits ADE-6 mixer between them. For the receiver/transmitter switch, I chose an ADG1419 IC, which lacks the isolation of a more traditional RF switch but comes in a more convenient package. I solved the isolation problem by turning off the transmitter signal at the DDS board.

The demodulated, amplified signal returns to the noisy part of the box, where it is digitized by an Analog Devices AD7690 PulSAR (successive-approximation-register) ADC sampling as fast as 100,000 samples/sec (**Figure 5**). This pin-compatible series of converters lets me select an optimal speed and SNR for my application without changing the PCB's design. The ADC board also contains a Xilinx XC95144XL CPLD to handle housekeeping and serial/parallel-conversion tasks, as well as to interface to DACs I didn't use for the design. Alternatively, I could have interfaced the ADC directly to the DSC through its McBSP (multichannel buffered serial port), but the ADC board was at hand.

The ADC board interfaces to the controller board through a 48-pin DIN connector containing the DSC's 16-bit data bus along with a few address and strobe lines. The DSC uses DMA to transfer one 262,144-sample NMR scan of ADC data into the external SRAM. Between scans, it adds the data from the last scan to another area of external SRAM that stores the accumulated scans. When the host decides that the instrument has accumulated enough scans, it reads out the accumulated data over the USB interface.

Note that USB is not an isolated protocol. As soon as you plug in a USB cable, you've connected your instrument's ground to your PC's ground, with predictable results. It's therefore a good idea to consider adding isolation, or be ready to specify an external isolator. Also, the FT245 chip that I used for the USB interface has a virtual-communication port that dramatically simplifies the host software's burden, allowing control through MathWorks' Matlab and National Instruments' LabView, for example. A trade-off exists, however, in that the host periodically sends packets to the USB to poll the status of the instrument's USB chip. In sensitive instruments, this added activity can noticeably affect the noise floor. One solution is to force the host application to close the communication port during the noise-sensitive acquisition phase and then reopen it for the data-transfer phase.

PROTOCOL PARTICULARS

My instruments always include a diagnostic ASCII protocol comprising simple two-character commands and heavy use of punctuation. Commands contain one or two alphabetic characters followed by an optional numeric argument and a semicolon, and spaces are ignored. For example:

- To set the transmit pulse width to 50 µsec, the host sends "PW 50;"
- If the instrument understands the command, it sends a confirmation: "PW 50!"
- If the command isn't in the instru-

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ment's vocabulary or if the argument is out of range, it returns "PW 50?"
• If the host wants to read the current setting of the transmitter pulse width, it sends the command in lowercase: "pw;"
• The instrument returns "pw50!"

This protocol is inappropriate for efficiently transferring large blocks of data, and usually gets supplemented or replaced as the host software is developed. Still, it allows you to control an instrument from any terminal emulator. I put the same protocol on the USB and asynchronous ports, with both ports always active, so I can use one for the main host interface and the other for a diagnostic port.

At the host end of the system chain, Changwook Min, a mobile-programming engineer at Massachusetts General Hospital's Center for Systems Biology, wrote the code to control the DMR-3 and analyze the returned data. He performed the initial development on an Apple Macintosh computer, using Objective-C under the Apple's Xcode 3.2.5 IDE (integrated device environment). He then ported the application to the iPhone 3G and iPad running iOS Version 4.2. Xcode has no native graphing or plotting framework, so Min used Apple's Core Plot.

REVISION: NOT TO BE

If I'd had a chance to clean up the design, I would turn the bottom three boards into one. I'd stick with the Delfino DSC, discard the CPLDs, and couple the PulSAR ADC directly to the DSC through the McBSP port. I'd either replace the DDS chips with a dual part or, more daringly, use a single DDS for the transmitting and receiving chains. After all, we don't acquire data while transmitting, so there's no reason why one DDS couldn't do both functions.

I'd optimize the RF power amps for the actual power; we were unsure of the power budget when we performed the initial design and, therefore, went a little overboard. I would also design the receiver path with cost in mind, replacing the second VGA (variable-gain amplifier) with something more appropriate.

Such a redesign will never happen, however. Once a concept is proven and the science is done, you either abandon the instrument or throw it "over the wall" to industry—to an engineering team that will undoubtedly start from scratch. EDN

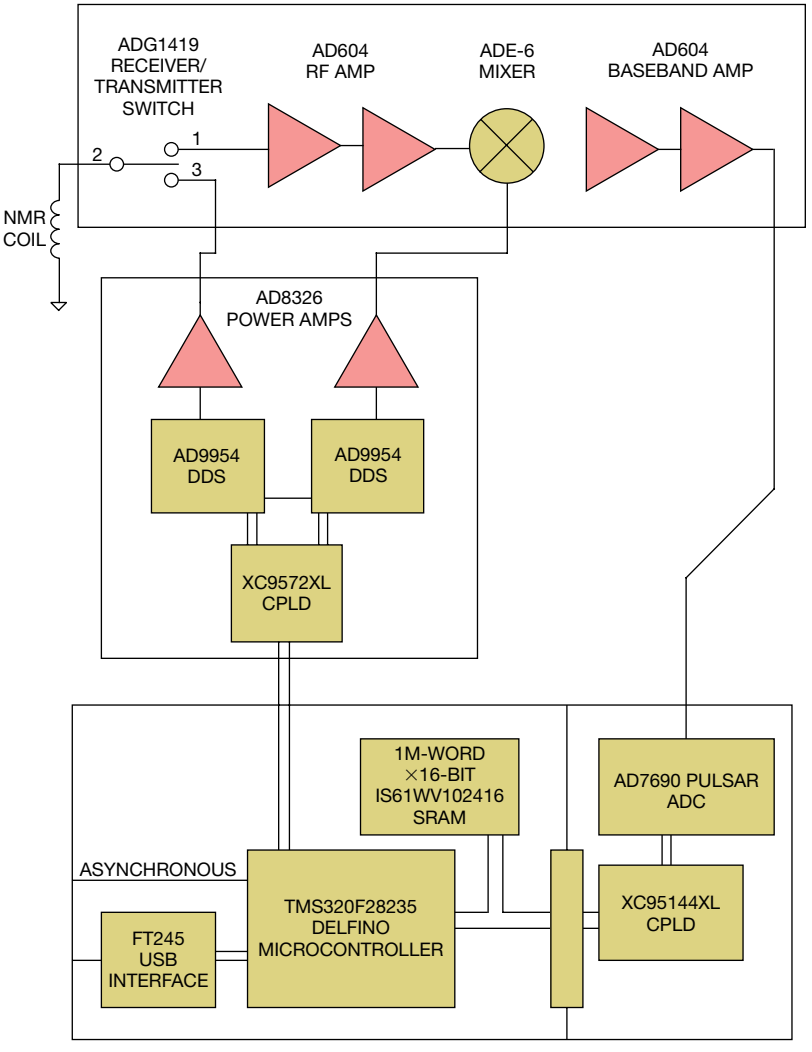

Figure 5 Signals take paths in the DMR-3 as they traverse the design's various circuits.

ACKNOWLEDGMENT

The author would like to thank Hakho Lee and his talented team at the Massachusetts General Hospital Center for Systems Biology, especially physicist Dave Issadore and programmer Changwook Min. Thanks also to Keith Brown of Harvard SEAS for his NMR tutelage, and to Al Takeda for photographing the DMR-3 viscera.

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AUTHOR'S BIOGRAPHY

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EDA TOOLS PAVE PATH TO

BY MIKE DEMLER • TECHNICAL EDITOR

A recent article (**Reference 1**) posed three questions regarding 3-D ICs: What are 3-D ICs, are they real, and what difference do they make? The answers to these questions may vary, but the semiconductor industry is increasingly adding a vertical—that is, stacked—alternative to traditional 2-D Moore's Law scaling (**Reference 2**).

Reducing the length of interconnects between ICs can make a big difference in performance, power, and package size in mobile-system applications—major drivers for 3-D ICs. Combining a mobile-processor die with a separate memory chip is a natural development for a 3-D structure. For example, Samsung Electronics recently introduced a 3-D IC, which the company stacks with a memory chip that connects using TSVs (through-silicon vias)—vertical, metallized holes in the silicon die that create connections on both the top and the bottom of a chip (**Figure 1**). TSV technology enables a wide I/O-memory interface, reducing power by as much as 75% versus other approaches as a result of the lower load capacitance of interconnect and I/O circuits.

Tezzaron Semiconductor, which specializes in memory products, 3-D-wafer processes, and TSV processes, stacks chips in three layers by using a wafer-bonding technique that employs copper supercontacts similar to the method the US Mint uses to make quarters in a copper-nickel-clad process. Tezzaron's Super-8051 microcontroller with stacked memory consumes 90% less power than a typical 8051 microcontroller because it has no off-chip I/O. It does not, however, allow manufacturers to probe wafers before bonding because probe marks can cause defects.

To mitigate some of the challenges of 3-D stacked ICs, many companies are taking an intermediate step—2.5-D—to connect dice with a passive silicon interposer (**Figure 2**). Many industry participants, including Mentor Graphics Chief Executive Officer Walden Rhines, see the 2.5-D approach as providing a long transitional ramp to 3-D ICs (**Reference 3**). Rhines believes that 2.5-D approaches will be around longer than many people expect because the approach is more evolutionary than revolutionary.

Xilinx has also taken this approach in its new 2.5-D SSI (stacked-silicon-interconnect) FPGAs, including the Virtex-7 XC7V2000T, which integrates four FPGA dice with the equivalent of 2 million logic cells, 46,512 kbits of block RAM, 2160 DSP slices, and 36 10.3125-Gbps Xilinx GTX (gigabit-transceiver-extension) transceivers (**Figure 3**). By stacking the dice on a passive silicon interposer, Xilinx enables more than 10,000 interconnects between the FPGAs. Showing again how 2.5- and 3-D make a difference in power and performance, Xilinx achieved a better-than-two-orders-of-magnitude improvement in I/O bandwidth per watt with SSI versus other approaches, says Ivo Bolsens, Xilinx's chief technology officer.

Your choices of EDA tools to support a new 3-D-IC project can make a difference in how you approach your design. Although you may be able to adapt your current 2-D-IC tools, you might also benefit by adding some technology targeting the challenges of 3-D design. Most of the major EDA vendors are taking a cautious wait-and-see approach to 3-D ICs by gradually adding features to their 2-D tools. Meanwhile, several

IMAGE: ISTOCKPHOTO.COM

GOING VERTICAL ENABLES HIGHER-DENSITY CIRCUITS WITHOUT SCALING TO SMALLER PROCESS GEOMETRIES.

3-D ICs

smaller EDA vendors are building tools focusing on 3-D design. The Tezzaron 3-D PDK (process-design kit), for example, combines new and established tools that will help you move your design method to 3-D.

TSVs' DOWNSIDE

The development of EDA tools for 3-D ICs must begin with TCAD (technology-computer-aided design) for modeling the physical characteristics of the TSV, according to Marco Casale-Rossi, product-marketing manager for Synopsys' implementation platform. The company's Silicon Engineering Group has undertaken this activity with several selected partners. Designers must address the fact that TSVs induce stress in the active silicon area near the via cut, which can potentially interfere with circuit behavior. At process geometries of 28 nm, the "keep-out zone"—the area around a TSV in which you cannot insert active circuitry—can consume an area equivalent to approximately 5000 transistors. Placing a large number of TSVs on a chip with the associated keep-out zones can result in a large amount of unusable die area, says Casale-Rossi. Synopsys recently filed for a patent for technology to address TSV-induced stress. The technology goes beyond TCAD software to IP (intellectual property), which Casale-Rossi predicts will contribute to stress-mitigation methods in 3-D-IC fabrication (**Reference 4**). The company has also filed patent applications for RLC (resistance/capacitance/inductance) modeling and extraction in 3-D ICs (**references 5** and **6**).

Synopsys bases the development of 3-D-IC physical-implementation tools on its 2-D place-and-route tools.

AT A GLANCE

- Manufacturers are introducing stacked-die ICs with memory on top of CPUs and multiple FPGAs with tens of thousands of connections that route through silicon interposers.
- TCAD (technology-computer-aided-design) tools enable designers to evaluate the effect of the stress that vertical TSVs (through-silicon vias) induce in 3-D ICs.
- Floorplanning and physical-verification tools are adding awareness of multiple die layers to account for TSVs.
- Custom physical-design tools for 3-D-IC design add the capacity to handle larger design databases.
- System-level 3-D-design tools enable engineers to evaluate design partitioning in stacked-die prototypes.
- Testing of 3-D ICs requires development of new methods for BIST (built-in self-test) and scan insertion.

Synopsys is developing a 2.5-D tool for designs that connect multiple flip-chips with microbumps through a silicon interposer. An emerging 3-D-IC design flow will be TSV-aware at every step of current flows—from synthesis and placement and routing to extraction, physical verification, and timing sign-off for digital designs (**Figure 4**).

ADDING FLOORPLAN LEVELS

Because no currently available EDA tools support automated placement and routing of TSVs, you must manually add tools using existing tools for 2-D-IC design. According to Dave Noice, Cadence Fellow, modifying 2-D tools and design databases to support the concept of 3-D ICs involves many challenges. For example, in 2-D designs the first metal, or metal-1, layer represents the lowest interconnect layer on an IC, but 3-D ICs change that placement by adding backside metal to make connections through TSVs.

Designers have previously been able to use Cadence's Encounter digital implementation tools to automatically route flip-chips, with 45° routing for bumps and I/Os. Cadence also enhanced that feature to provide support for I/O routing on both the top and the bottom of a die. After you add TSVs to a chip during the floorplanning and placement stage, the next challenge you will face is assigning connections. A routing tool must be able to assign a connection and optimize wire length through the TSVs to backside bumps. Some users mistakenly believe that a router can place the TSVs, says Noice, but designers can use routers only to make the connections. In a stacked-die configuration, designers' flexibility constrains floorplanning—whether they are adding TSVs to a new ASIC or modifying a design for use in a 3-D package.

For 3-D-IC designs, Cadence's floorplanning tools treat the problem as if it were a normal hierarchical 2-D design. The tools treat each die as a separate subblock. For example, if a given manufacturing process stacks memory dice, die "owners" can see the vertical-connection interface for design optimization but can make edits only on their side of the TSV stack.

Magma Design Automation is extending its Hydra floorplanning tool to automate 3-D designs by treating a 3-D chip as a set of 2-D blocks for physical implementation. According to Patrick Groeneveld, PhD, chief technologist at Magma, partitioning a 3-D design into the constituent 2-D components can give rise to a number of new issues, such as design partitioning, TSV assignment, interfaces across dies, power and ground distribution, and the associated IR drop and temperature analysis.

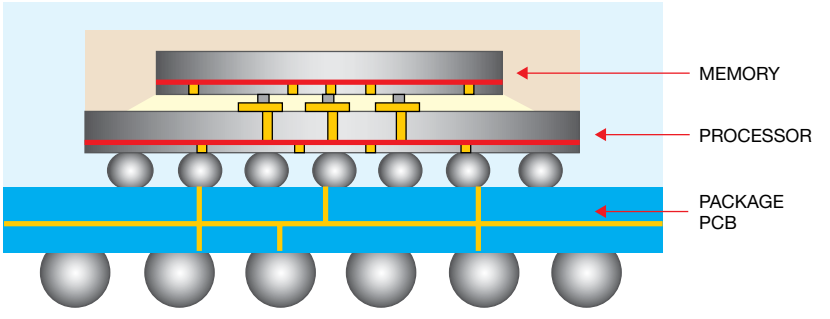
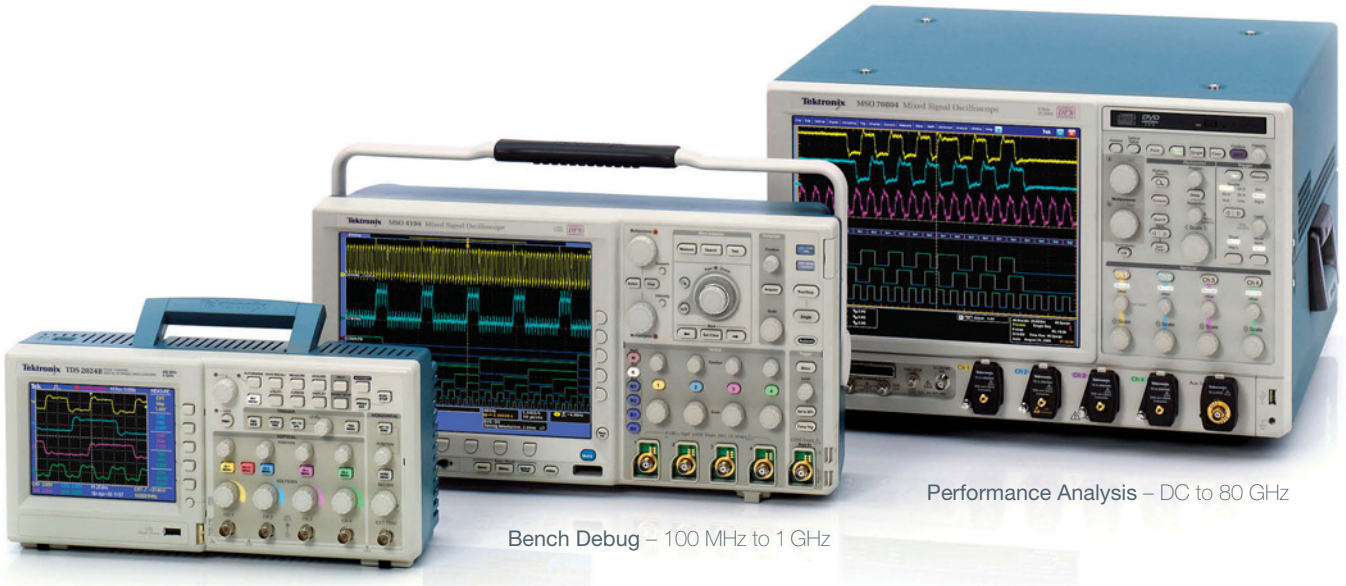


Figure 1 Samsung Electronics stacks its new 3-D IC with a memory chip that connects using TSVs.

CUSTOM TOOLS

The market for 3-D-IC design tools has been too small to attract investment by the big EDA companies, according

The World's Standard.



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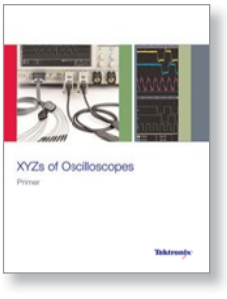

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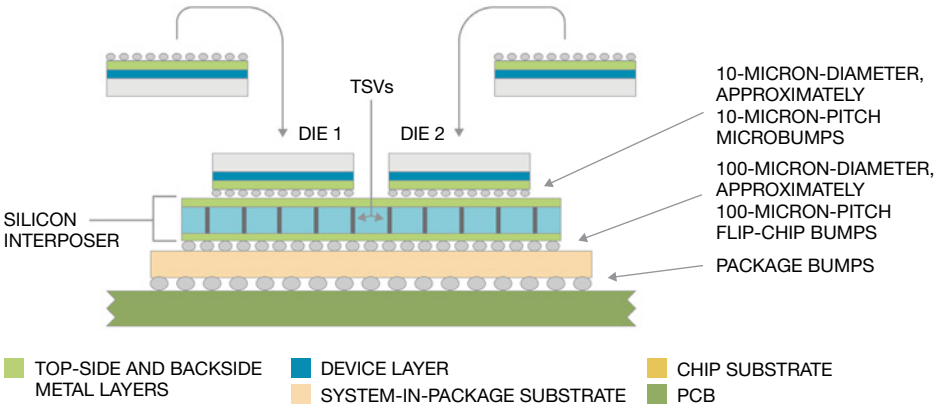

Figure 2 ICs using a 2.5-D approach use a combination of flip-chips with TSVs for backside connections, with microbumps and a silicon interposer to combine multiple dice on a common substrate (courtesy Cadence Design Systems).

to Mark Mangum, sales and marketing manager at privately held EDA company Micro Magic. The company has been working on the Max-3D layout tool for the last four years, with 3-D design patents from one of its development partners (**Reference 5**). Conventional layout tools cannot handle the traditional approach for 2-D design—organizing all the disparate data into one huge file, says Mangum. Max-3D, in contrast, allows you to maintain technology files for each wafer level, with a separate file for the TSV interconnects (**Figure 5**). Engineering teams of processor and memory designers, which are common in projects for 3-D ICs, can work independently on their parts of the 3-D stack before final integration.

After assembly of the 3-D-IC database, you must verify your design by tracing the connectivity of the TSVs through the entire stack and perform complete DRC (design-rule checking) and LVS (layout-versus-schematic) checks. You must somewhat adapt the 2-D physical-verification tools, but Max-3D eases this process through its integration with Mentor Graphics' Calibre DRC and LVS tools. Micro Magic is also working with Magma to integrate the company's Quartz LVS and DRC tools into Max-3D. Magma's Groeneveld says that future enhancements to Quartz will enable users to work directly with the multiple process descriptions that are necessary for 3-D ICs. With Quartz LVS, you can check each of your 2-D chips, as well as the 3-D interconnections between them, in a single run (**Figure 6**). You specify the number and order of layers, the interconnect material, and other physical parameters of your design in a 3-D technology file. You then perform a TSV-aware extraction of your 3-D IC's connectivity, using the debugging environment in Quartz to analyze any LVS mismatch.

Magma intends to add 3-D-DRC features to Quartz by working with customers and manufacturers to define the rules, design, and library information that will be necessary to verify designs with TSVs. According to Groeneveld, Magma is also working on several other projects for 3-D ICs, including adding the ability for users to visualize and edit multiple dice at once in the Titan custom-IC layout editor with built-in Quartz DRC and LVS checking.

Designers are typically reluctant to switch tools or alter their 2-D flows, so if they can make a conventional IC-layout tool work for their 3-D designs, they will do it, says Micro Magic's Mangum. At some point, however, conventional tools can't handle the size of the required database. The company has demonstrated Max-3D on designs with as many as 1 trillion transistors, and designers have used the tool to develop designs with databases as large as 60 to 80 Gbytes. Max-3D complements popular 2-D-IC-layout tools, such as Cadence's Virtuoso, by taking over 3-D-design tasks when the database becomes too large. Micro Magic helps with design-flow integration and interoperability by providing full support for the Si2 (Silicon Integration Initiative) OpenAccess Coalition's OpenAccess database format, a community effort to provide interoperability, including unified data exchange among IC-design tools through an open-standard data API (application-programming inter-

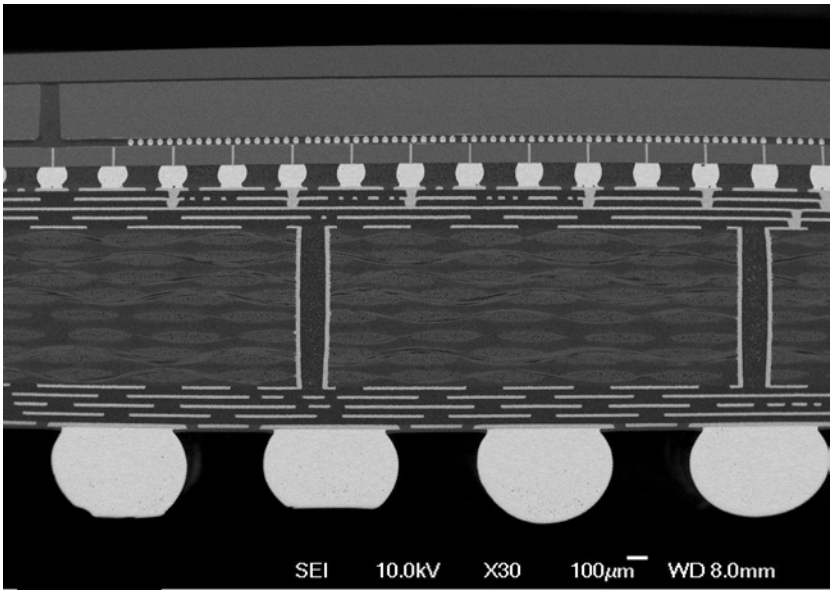

Figure 3 In a cross section of a 28-nm Virtex-7 device, TSVs connect the microbumps (dotted line at top) through a silicon interposer (courtesy Xilinx).

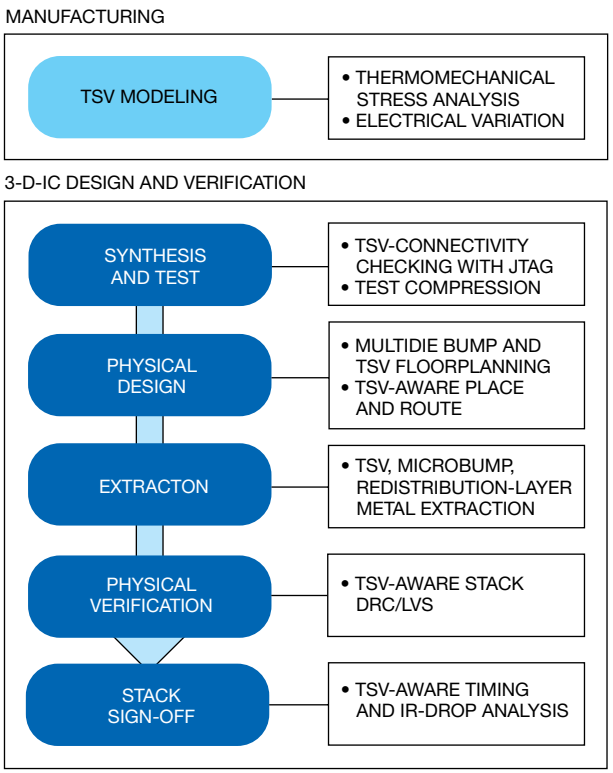

Figure 4 Synopsys' view of an emerging 3-D-IC design flow involves adding TSV awareness to available 2-D tools.

face) and reference database supporting that API for IC design.

DESIGN TOOLS FOR 3-D PARTITIONING

Manufacturers are now offering tools for early planning and partitioning of 3-D ICs. For example, Atrenta offers RTL (register-transfer-level) prototyping technology in its SpyGlass-Physical Advanced tool for early planning and partitioning of 3-D ICs. The 2-D Atrenta SpyGlass tool enables designers to start physical-implementation feasibility analysis early in the design cycle when RTL may still be incomplete. You can visualize and evaluate multiple floorplan configurations, analyze implementation feasibility, select appropriate silicon IP, create physical partitions, and generate implementation guidance for IP and SOC (system-on-chip) implementations (**Figure 7**).

For 3-D ICs, Atrenta has taken the place of earlier efforts at the now-defunct Javelin Design Automation, which the company performed in collaboration with IMEC and Qualcomm (**Reference 6**). Atrenta has recently opened an R&D facility that will focus on developments in 3-D technology and advanced power-reduction techniques.

When IMEC and Javelin started the 3-D-IC work with Qualcomm, the first challenge was to be able to understand a design from a system level. "We had to figure out a way to partition a design across multiple levels and understand the impact of the TSVs on the entire design so that we could do some early floorplanning," says Pol Marchal, principal scientist at IMEC. IMEC was easily able to convert Atrenta's SpyGlass for use on 3-D designs, he says.

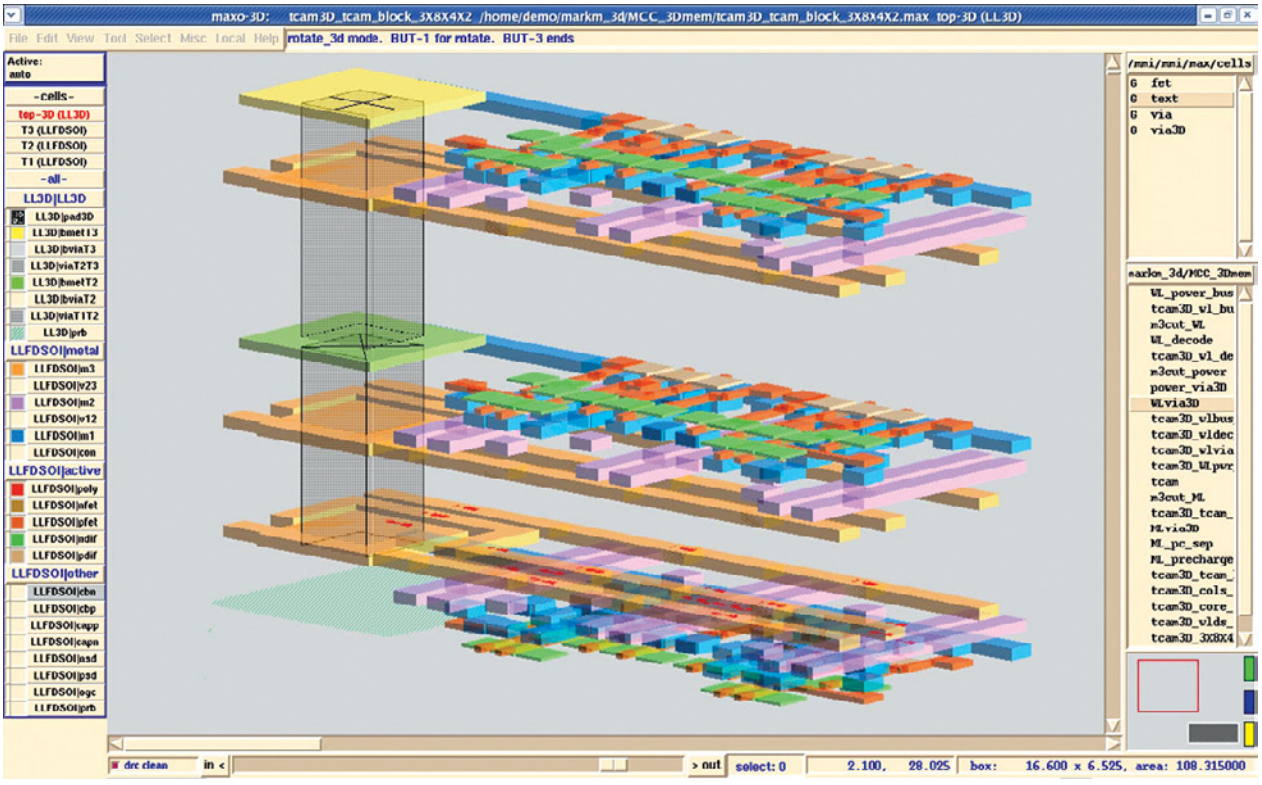

Figure 5 The Max-3D tool incorporates features for 3-D-design methods, so you can organize and manage design data for every wafer level in a stacked design.

To enable design exploration and optimization in a 3-D design, according to Atrenta Fellow Ravi Varadarajan, you need a tool that can understand stacked-die configurations and process technologies. At the beginning of the design process, which Atrenta refers to as logical pathfinding, you must capture designer intent. Atrenta treats each die as a unique 2-D partition, basing all of its work on the OpenAccess API and database format.

Atrenta is also collaborating with IMEC on an alpha project that will allow designers to feed the results of floorplanning into a thermal-simulation engine. Commercial tools, such as Gradient's HeatWave, are available for thermal analysis of 3-D ICs (**Reference 7**). By developing its own tool, IMEC was able to easily calibrate thermal-analytical models with measurement data from its test devices. IMEC also has developed its own tool for analysis of mechanical stress that works with Atrenta's tools, and Marchal agrees with Synopsys regarding the importance of assessing stress effects early in a 3-D design.

Start-up Monolithic 3D Inc focuses on developing tools and manufacturing techniques for 3-D ICs. The company is working on the 3DSim system-level design-planning simulator for use for 2- and 3-D ICs. It processes inputs, such as transistor parameters, interconnect materials, the number of 3-D stacked layers, and packaging, to develop models for signal wires, logic gates, power distribution, heat removal, and clock distribution. You can also use 3DSim to explore design trade-offs for 3-D ICs. Monolithic offers the tool in open-source Java that can be run from the company's Web site.

TESTING THE 3-D STACK

Testing is another challenge for 3-D stacked die. Mentor Graphics is addressing the challenge and identifies three issues in testing of 3-D ICs: ensuring known-good die, providing access to retest dice after packaging them in a stack, and providing access to the TSVs that interconnect the dice inside the package, according to Stephen Pateras, product-marketing director for the company's silicon-test products. Some parts in single-chip packages will inevitably fail to meet specifications because of the cost and complexity of thorough at-speed wafer-level testing. The yield loss becomes part of the cost equation for product engineers, who must determine whether ROI (return on investment)

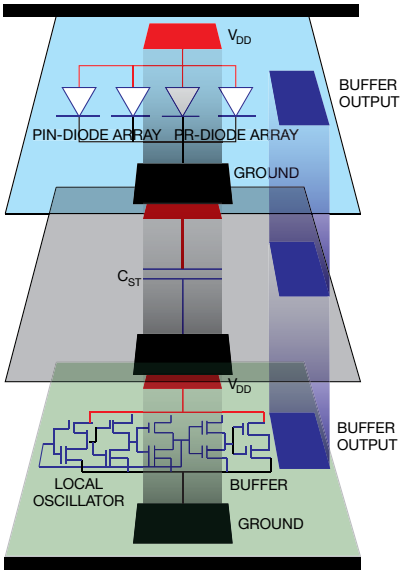

Figure 6 Quartz LVS lets you check 2-D chips and the 3-D interconnections between them in one pass.

will be sufficient to justify the additional cost of prepackaged-die testing. For 3-D ICs, these challenges change the economics of test because a failure in one die means you must also discard the good dice.

Mentor Graphics' Tessent silicon-test platform provides tools for embedded BIST (built-in self-test) of all parts of a die, including logic, memory, and mixed-signal and high-speed I/O. Using a BIST approach frees you from worrying about access, other than through a low-speed JTAG (Joint Test Action Group) IEEE-1149.1 port.

IEEE Standard 1149.1-1990 defines allowable built-in circuitry for ICs to assist in the test, maintenance, and support of assembled PCBs (printed-circuit boards). The circuitry includes a standard interface through which the system communicates instructions and test data. It defines a set of test features, including a boundary-scan register, so that the component can respond to a minimum set of instructions to assist with testing of assembled PCBs.

With BIST and ATPG (automated test-pattern generation), you can perform hierarchical at-speed testing in parallel for various blocks inside a chip. This approach is not new, but it is critical for 3-D ICs because the intermediate dice in a stack have no connection to the outside world. As a result, you have no access to scan-test inputs and outputs. This constraint places a new requirement on 3-D design: You must reroute test access to the TSVs by using so-called test elevators. IMEC has proposed this architecture to the IEEE as an enhancement of the 1149.1 specification. With test elevators, you must incorporate routing and logic to switch 3-D connections into test mode throughout a die stack. Design requirements change because this approach involves daisy-chaining test logic within a stack. With test elevators, you may employ multiplexer circuitry on one die to pass test patterns from another die. You might also need to combine test patterns from multiple dice. The new 3-D capabilities in Mentor Graphics' Tessent tools enable you to insert test elevators, along with the logic that you may need for retiming test sequences that originally targeted use within a die, to allow retest by sending patterns through a TSV.

According to Pateras, Tessent treats the 3-D-die-stack problem in a way that resembles 2-D hierarchical test within a die. Hierarchical test generation independently treats each block in a die and resequences patterns at the top level. You would use "gray-box" test techniques—having knowledge of internal data structures and algorithms for designing test cases. This approach would be used for multiple dice, rather than for IP blocks within a die, so that a Verilog netlist now covers the entire package.

Designers can use Tessent's MBIST (memory-BIST) controller to perform a

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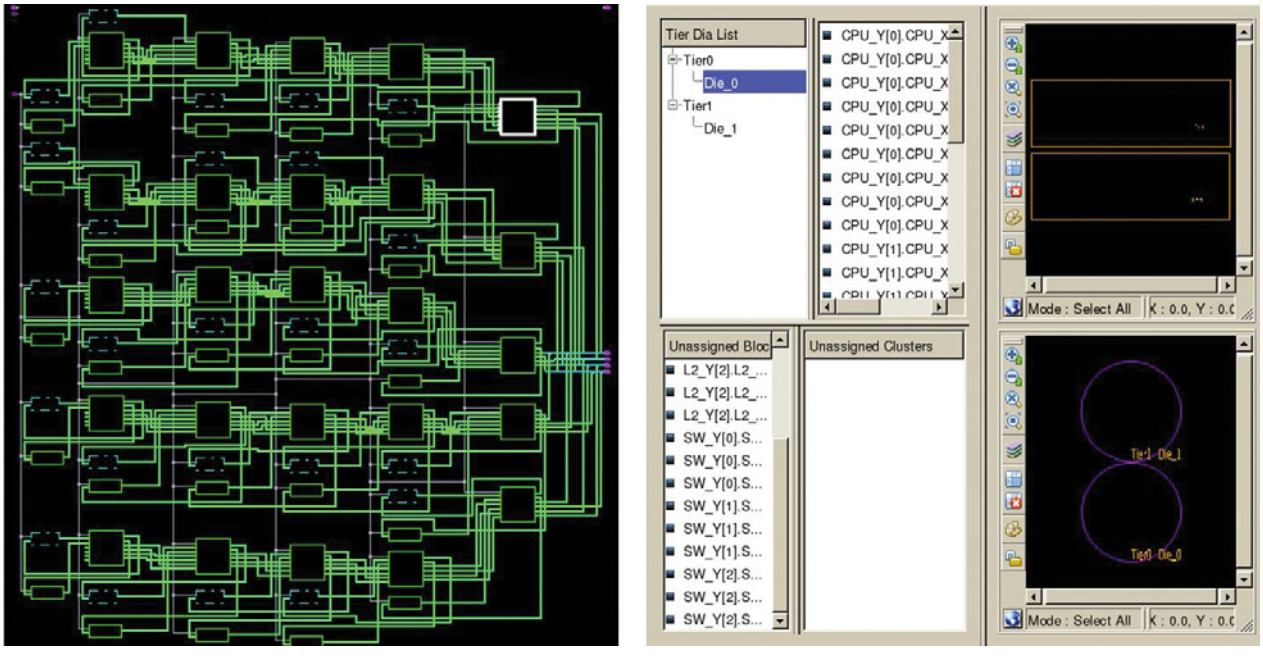

Figure 7 In Atrenta's 3-D pathfinding tools, each node in the array comprises a CPU core, with a switch to provide the interconnection to adjacent nodes, a network on chip, memory, and Level 2 cache memory. The 3-D partitioning allows you to explore which components of the array you can move to another die and how that decision would affect performance.

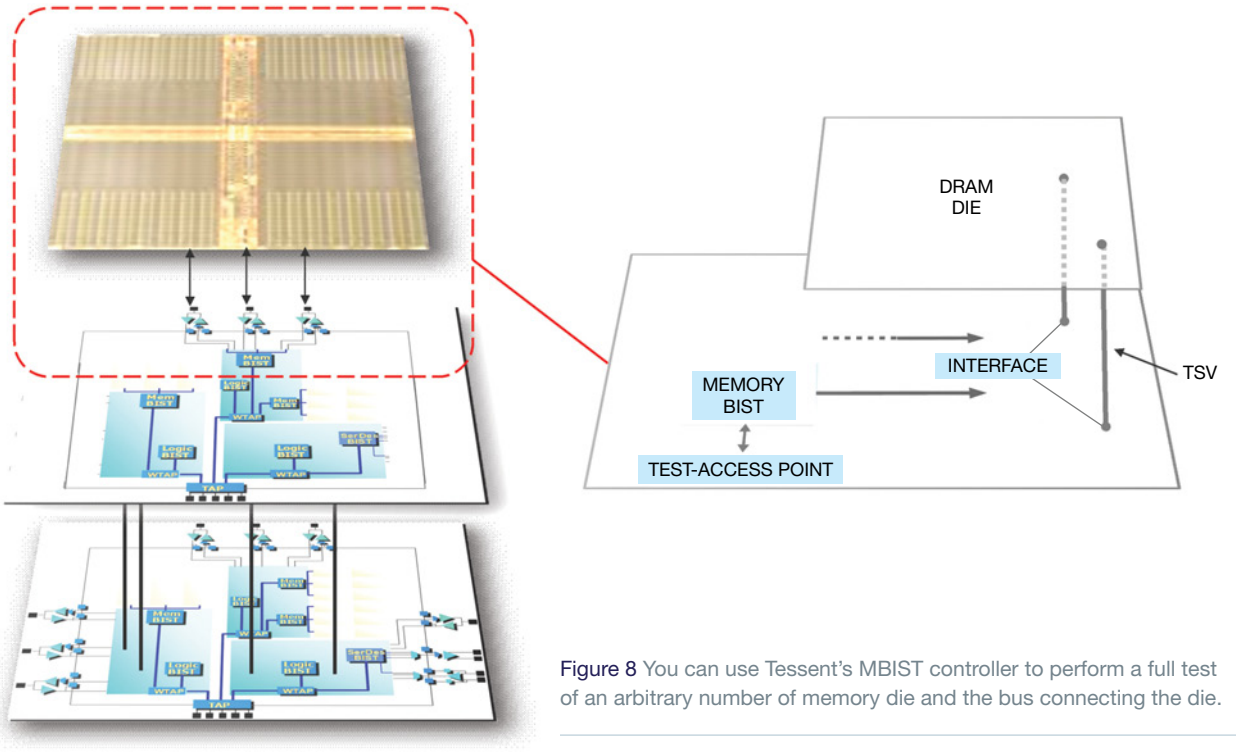

Figure 8 You can use Tessent's MBIST controller to perform a full test of an arbitrary number of memory die and the bus connecting the die.

full test of an arbitrary number of memory dice and the bus connecting them (**Figure 8**). The company's 3-D features allow the integration of MBIST circuitry on a logic chip, separate from the DRAM die. You can use the shared-bus capability to support multiple memory dice and apply postsilicon programmability to support design changes. This approach allows you to support variations in the stacked memory on a logic chip for different applications and change test requirements as the size or performance specifications of memory change. You can also test logic on one die that connects to logic on another die through TSVs. This feature provides both horizontal-2-D and vertical-3-D scan-insertion methods.

The challenges that must be addressed for testing 3-D ICs fall into three categories, according to Erik Jan Marinissen, principal scientist for 3-D-IC test at IMEC. First, you must determine what requires testing and where and when in the manufacturing cycle to test it. You must then address issues that relate to the new defects that 3-D-processing steps and TSV interconnects can introduce. The third challenge is test access. IMEC's work on testability tools for 3-D ICs includes collaboration with Cadence, which IMEC and Cadence at press time had planned to demonstrate at the 2011 Design Automation Conference, scheduled to take place this month in San Diego. Marinissen is also the working group chairman for the IEEE Standards Association's Project P1838: Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits. In a white paper on the challenges of 3-D-IC design, Cadence states that more empirical data is necessary to determine the need for new fault models (**Reference 8**). Although 2-D-IC defects, such as opens, shorts, static, delay, and bridging faults, may be adequate data for 3-D ICs, 3-D technology requires a new method for mapping TSV defects to the known fault types. To meet 3-D controllability and observability goals, Cadence also indicates that intelligent allocation of DFT (design-for-test) resources across multiple dice is essential. EDN

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BY ALAN SY • SILICON LABORATORIES

Designing IR gesture-sensing systems

USE OR COMBINE POSITION- AND PHASE-BASED SENSING TECHNIQUES TO DESIGN ACCURATE IR GESTURE-SENSING SYSTEMS.

Touchless user interfaces are an emerging technology for embedded electronics as developers seek to provide innovative control methods and more intuitive ways for end users to interact with electronics products. Active IR (infrared) proximity-motion-sensing technology can solve this human-interface design challenge.

Thanks to the advent of highly integrated proximity/ambient-light sensors, implementing motion sensing using IR technology is now easier. The two primary methods used to enable gesture sensing are position-based and phase-based sensing. Position-based gesture sensing involves finding gestures based on the calculated location of an object. Phase-based gesture sensing is based on the timing of the changes in signals to determine the direction of an object's motion. Both technologies are complementary enablers of IR gesturing applications, such as page turning for e-readers, scrolling on tablet PCs, and navigating GUIs (graphical user interfaces) in industrial-control systems.

HARDWARE CONSIDERATIONS

Although touchless-interface applications primarily involve gestures made by a human hand, gesture-recognition concepts can also apply to other targets, such as a user's cheek. Application and system constraints dictate IR gesture-sensing range requirements. Object reflectance is the main measurable component, and a hand is the most common detectable object. A hand can achieve gesture sensing up to 15 cm away from the proximity sensor. Fingers, with dramatically lower reflectance than hands, can achieve gesture sensing at a range of less than 1 cm for thumb-scroll applications.

The general guideline for designing a gesture-sensing system with multiple LEDs (light-emitting diodes) is to ensure that there is no "dead spot" in the middle of the detectable area. When a target is placed above the system and is not detected, the target is in a reflectivity dead spot. To avoid dead spots, the LEDs must be placed such that the emitted IR light can reflect off the target and onto the sensor from the desired detection range (**Figure 1**). The most likely area for a dead spot is directly above the sensor, between the two LEDs. The two LEDs are placed as close to the edge of the target as possible to provide feedback in the middle while maintaining enough distance between the LEDs so that the target can be detected when the finger or hand moves left or right.

The location and reflectance of the target in relation to the system are also important. Note that the proximity sensor in **Figure 1** is located under the palm of the hand and in the middle of the finger. The fingers are poor focal points for hand-detection systems because light can slip between the fingers. The shape of the fingers also results in unpredictable measurements. For a finger-detection system, the tip of the finger is curved and reflects less light than the middle of the finger.

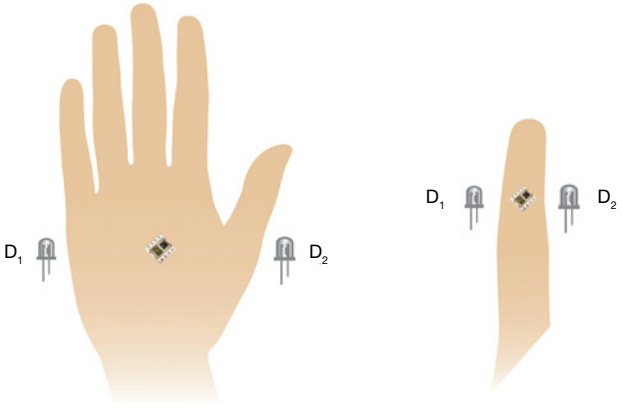


Figure 1 Spacing of the two LEDs depends on whether you are trying to sense hand movement or finger movement.

POSITION-BASED GESTURE SENSING

The position-based motion-sensing algorithm involves three primary steps. The first step is the conversion of the raw data inputs to usable distance data. The second step uses this distance data to estimate the position of the target object, and the third step checks the timing of the movement of the position data to determine whether any gestures have occurred.

The proximity sensor outputs a value for the amount of IR light that the IR LEDs reflect. These values increase as an object or a hand moves closer to the system and reflects more light. Assume that a hand is the defined target for detection. The system can estimate how far away the hand is based on characterization of the PS (proximity-sensing) feedback for a hand at certain distances. For example, a hand approximately 10 cm away yields a PS measurement of 5000 counts, so subsequent PS measurements of 5000 counts mean that a similarly reflective hand is approximately 10 cm away from the system. Taking multiple data points at varying distances from the system helps you interpolate between these points and creates a piecewise equation for the conversion from raw PS counts to a distance estimation.

Each LED in a system with multiple LEDs has a different PS feedback for each hand distance, so each LED will need an inde-

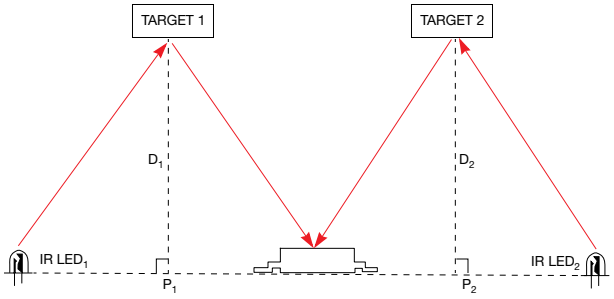


Figure 2 The sensed strength of the IR signal allows you to estimate the distance to a target.

pendent counts-to-distance equation. For a two-LED system, each LED must be characterized with a target suspended over the midpoint between the LED and the sensing device (**Figure 2**). When Target 1 is suspended over the sensing device and LED_1, the measured feedback will correlate to a distance, D_1, above the system. The same is true for Target 2, LED_2, and D_2.

The next step is to estimate the target's position using the distance data and the formula for the intersection of two circles. An LED's light output is conical; for this approximation, however, it is considered to be spherical. With the LEDs on the same axis, the intersection of these two spheres can be considered using equations for the intersection of two circles.

When a target is suspended over the middle of a system, D_1 and D_2 are the estimates of the distance from points P_1 and P_2 to the target above the system (**Figure 3**). Think of D_1 and D_2 as the radii of two circles; the intersection of these two circles is the location of the target.

Figure 4 is an expanded version of **Figure 3**, in which the measurements A and B label the location of the target along the axis between points P_1 and P_2. The distance measurements D_1 and D_2 have been renamed R_1 and R_2 to indicate that they are now considered radii. The value of A is the location of the object along the axis between P_1 and P_2. A negative value is possible, indicating that the target is on the left side of P_1. The distance to the target is a function of these variables, as the following **equations** show: $D=A+B$, and $A=(R_1^2-R_2^2+D^2)/2\times D$.

With the positioning algorithm in place, keeping track of timing allows the system to search for and acknowledge gestures. The entry and exit positions are the most important considerations for hand-swiping gestures. A left swipe occurs if the hand enters the right side with a high A value and exits the left side with a low A value. This scenario assumes that the entry and exit transpired within a defined time window. If the position stays steadily in the middle area for a set period, this gesture can be considered a pause gesture.

The system must keep track of the time stamps for the entry, exit, and current positions of the target in the detectable area. You can easily recognize most gestures with this timing and position information. Timing will need to be custom-tuned for each application and each system designer's preference.

PHASE-BASED GESTURE SENSING

With phase-based gesture sensing, the location of the target is never calculated. This method involves looking solely at the raw data from the proximity measurements and identifying the timing of the changes in feedback for each LED. The maximum feedback point for each LED occurs when a hand is directly above that LED. If a hand is swiped across two LEDs, the direction of the swipe can be determined by looking at which LED's feedback rose first.

When a hand is swiped left over a three-LED system, it crosses over D_2, then D_3, and then D_1 (**Figure 5**). The sensing algorithm recognizes the rise in feedback for D_2 and records the time stamp for this rise. The algorithm then detects the same rises for D_3 and D_1 with a later time stamp than the one before it. The algorithm also can detect the return of each LED's measurement to the no-detection state and can record a time

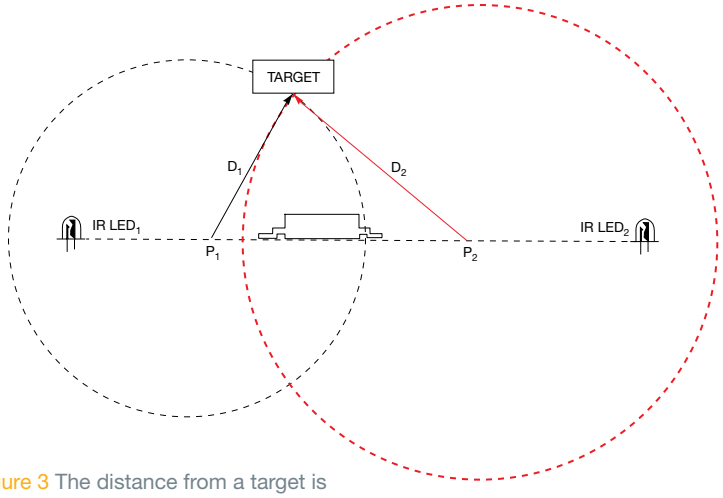


Figure 3 The distance from a target is a function of the intersecting radii of the two circles.

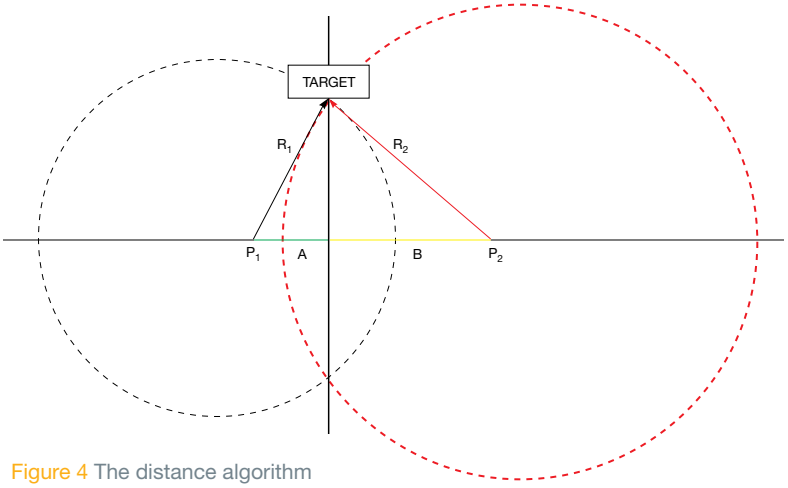


Figure 4 The distance algorithm solves the equation employing these definitions.

stamp for this event. In this case, D_2 returns first to a normal state, then D_3, and then D_1.

For up and down gestures, D_1 and D_2 rise and fall simultaneously, with D_3 coming either before or after D_1 and D_2 for the up or down gesture. If a hand approaches the system directly from above and then retracts to indicate a "select" gesture, all three channels rise and fall at once.

Figure 6 shows the signal responses of the right, left, down, and up gestures, which appear as ADC counts versus time. The green line represents PS measurements using D_1, the purple line represents PS data from D_2, and the yellow line shows data from D_3. For a right swipe, D_1 spikes first, followed by D_3 and then D_2. For the up and down swipes, D_1 and D_2 spike simultaneously because the hand crosses these LEDs at the same time when swiping up or down.

ADVANTAGES AND DRAWBACKS

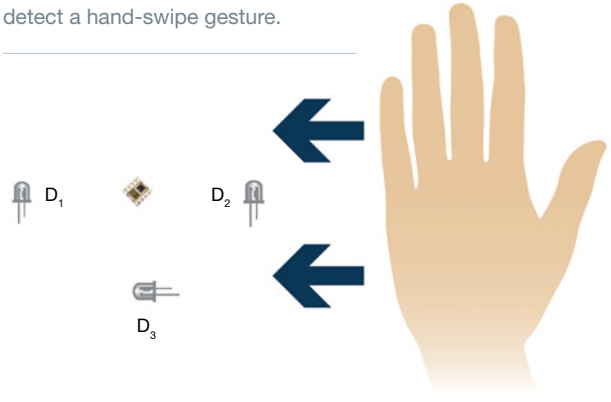
The position-based method can offer information on the location of the target, enabling ratiometric control of systems. For example, to scroll several pages through a book, you could suspend your hand over the right side of the detectable area rather than making several right-swipe gestures.

The main drawback of the position-based algorithm is the accuracy of the position calculations. The positioning algorithm assumes a spherical output from the LEDs, but in practice LED output is more conical than spherical. The algorithm also assumes uniform light intensity across the entire output of the LED, but the light intensity decays away from the normal. Another issue is that this algorithm does not account for the target's shape. A uniquely shaped target causes inconsistencies with the positioning output. For example, the system cannot tell the difference between a hand and a wrist, so it is less accurate when detecting any gestures involving movement that puts the wrist in the area of detection. The positioning algorithm is adequate for low-resolution systems that need only a 3×3 grid of detection, but the algorithm is not suitable for pointing applications. In short, this algorithm's output is not an ideal touchscreen replacement.

The phase-based method provides a robust way of detecting gestures in applications that do not require position information. Each gesture can be detected on either the entry or the exit from the detectable area, and the entry and exit can be double-checked to provide much higher certainty for each observed gesture.

The drawback of this method is that it provides no positioning information, meaning that it offers a more limited number of gestures that can be implemented than does the position-based method. The phase-based method can tell only the direction of entry and exit from the detectable area, so it does not recognize any movement in the middle of the detectable area.

Figure 5 Use three-LED hardware to detect a hand-swipe gesture.



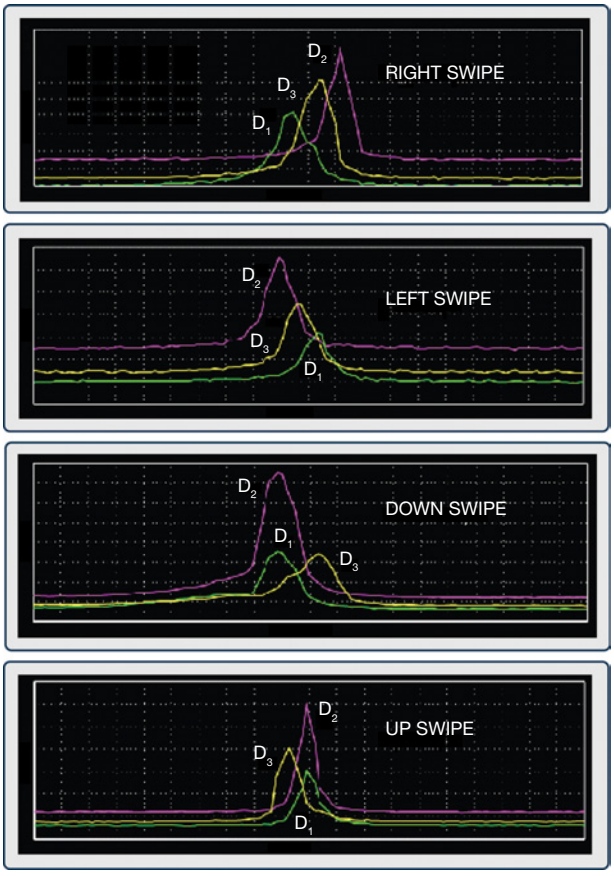


Figure 6 The intensity and timing data from hand swipes allow the algorithm to properly interpret the data.

COMBINING BOTH METHODS

Both position- and phase-based methods of gesture sensing can be implemented in concert to help mask and mitigate each method's inherent deficiencies. The position-based algorithm can provide some positional information for ratiometric control, and the phase-based algorithm can detect most gestures. These two algorithms together provide a robust approach for gesture-sensing applications. This dual-method approach requires more code space to implement and requires additional CPU cycles to process both algorithms. For a growing number of sophisticated human-interface applications, however, it may be well worth the computational trade-off to enable the next generation of gesture sensing. EDN

AUTHOR'S BIOGRAPHY

Alan Sy is an application engineer for Silicon Laboratories' human-interface products, specializing in infrared proximity-sensing products. He previously served as an application engineer in Silicon Labs' microcontroller-product group focused on sensorless motor control. Sy has a bachelor's degree in electrical engineering from the University of Texas—Austin.

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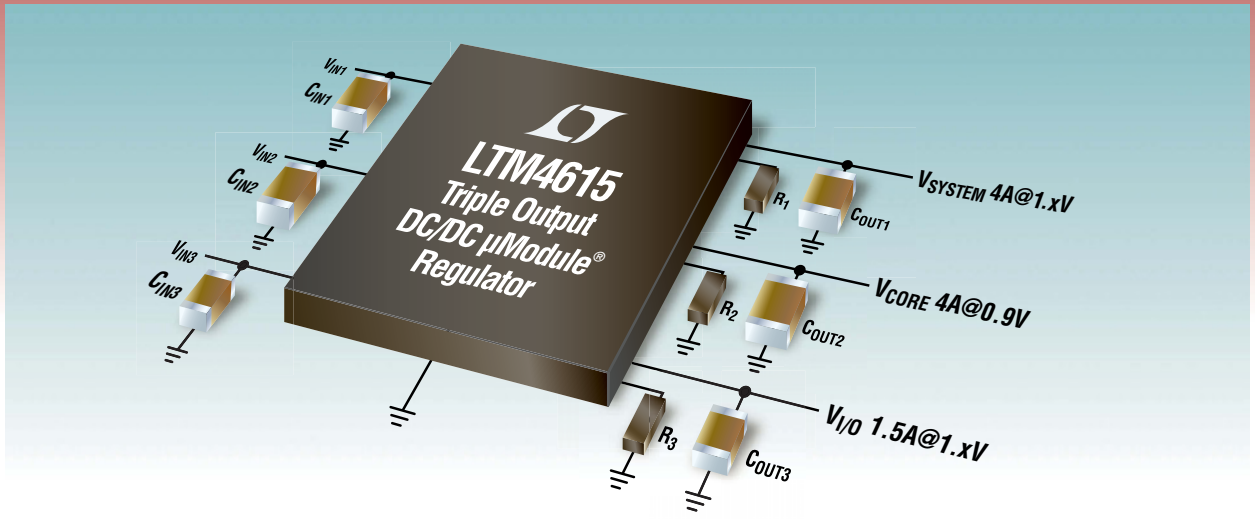

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Dual					
LTM4614	→ 4A → 4A	→ 8A Also see LTM4608A	V_{IN1}: 2.375V to 5.5V V_{IN2}: 2.375V to 5.5V	V_{OUT1}: 0.8V to 5V V_{OUT2}: 0.8V to 5V	
LTM4616	→ 8A → 8A	→ 16A	V_{IN1}: 2.7V to 5.5V V_{IN2}: 2.7V to 5.5V	V_{OUT1}: 0.6V to 5V V_{OUT2}: 0.6V to 5V	
High Voltage: ≤26.5V_{IN}					
LTM4619	→ 4A → 4A	→ 8A Also see LTM4601A	V_{IN1}: 4.5V to 26.5V V_{IN2}: 4.5V to 26.5V	V_{OUT1}: 0.8V to 5V V_{OUT2}: 0.8V to 5V	

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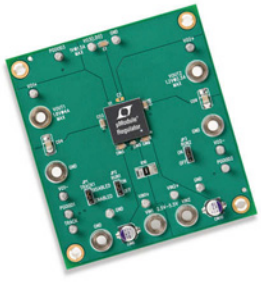

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designideas

READERS SOLVE DESIGN PROBLEMS

Potentiometer calibrates photodiode amplifier

Michael J Gambuzza, General Electric Energy, Billerica, MA

One of the nagging problems with optocouplers is that their light output varies with temperature, age, and CTR (current-transfer ratio). Thus, you may need to calibrate optocouplers to compensate for those variations. Using the circuit in **Figure 1**, you can calibrate an optocoupler's output using an up/down digital potentiometer. The amplifier circuit, a typical photovoltaic-mode device, uses IC_3, an Analog Devices (www.analog.com) AD5227 up/down potentiometer, which has 64 steps and powers up at midscale resistance. When a microcontroller output pin or another digital signal selects the device, the device's resistance changes with every clock pulse until the output voltage of the amplifier equals the maximum set reference voltage. The completion of the calibration cycle optimizes the amplifier's output for the optocoupler's CTR.

Driving the optocoupler's LED at a maximum dc current for a full-scale amplifier output puts the incident light at a maximum level. The circuit then asserts the calibration pulse for a time that depends on the AD5227's external clock rate. If the output of the amplifier is lower than the maximum reference

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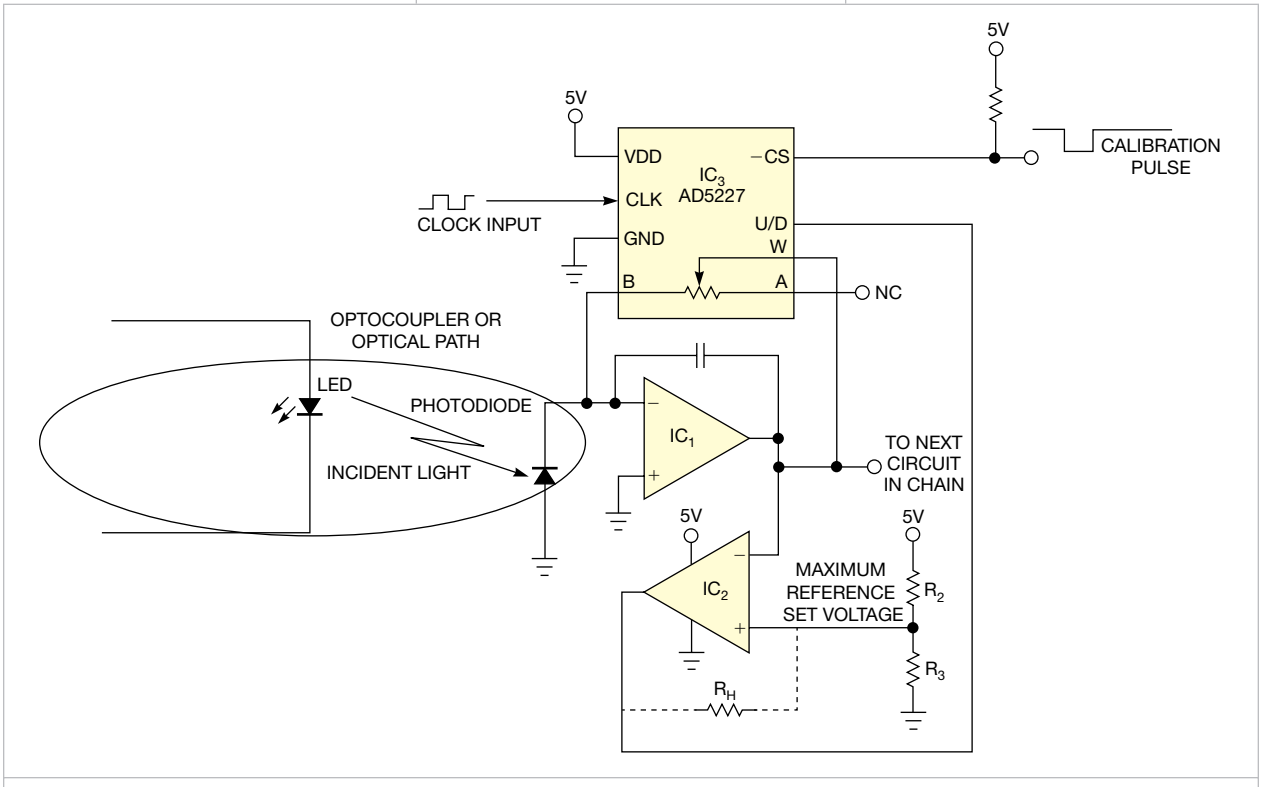

Figure 1 This circuit lets you calibrate an optocoupler's output using an up/down digital potentiometer.

voltage, IC_2's output goes high. This action increases the resistance from Pin W to Pin B, increasing the amplifier's gain. If the output of the amplifier is higher than the reference, IC_2's output goes low, causing the AD5227 to decrement the resistance, which reduces the gain.

For IC_2, use a comparator with built-in hysteresis or use external hysteresis, which resistor R_H provides. You can use this method for other applications besides optocouplers; for example, you can also apply it to lasers. Photoamplifier designs can be tricky, so make sure to carefully craft your amplifier's compensation, layout, and power-supply decoupling. EDN

Drive 16 LEDs with one I/O line

Zoran Mijanovic and Nedjeljko Lekic,
University of Montenegro, Podgorica, Montenegro

Over the last few years, several Design Ideas have described how to use just a few microcontroller I/O pins to drive many LEDs (**references 1** through **7**). The circuit in **Figure 1** can drive 16 LEDs with just one pin and two shift registers. You can use the circuit to drive long-dot-bar or two seven-segment-digit displays. Adding multiplexing to the same circuit enables it to drive eight seven-segment LED digits.

The microcontroller drives the shift registers' clock inputs. That signal also passes through an RC filter and drives data inputs A and B. A 100-kΩ resistor, R, and the A and B input pins' capacitances form the RC filter (**Figure 2**), producing time delay of approximately R×C×ln2=100 kΩ×(5 pF+5 pF) ×0.7=0.7 µsec.

To write a logic zero to the shift register, the microcontroller holds a low level for approximately 2 µsec, which is longer than the time delay. It then sets the signal to a logic one, or high, level. To write a logic one, the microcontroller holds the high level for longer than the time delay. The microcontroller then makes negative pulses of approximately 0.25 µsec, or two CPU cycles, which is shorter than the time delay and which doesn't change the logic level at the data inputs.

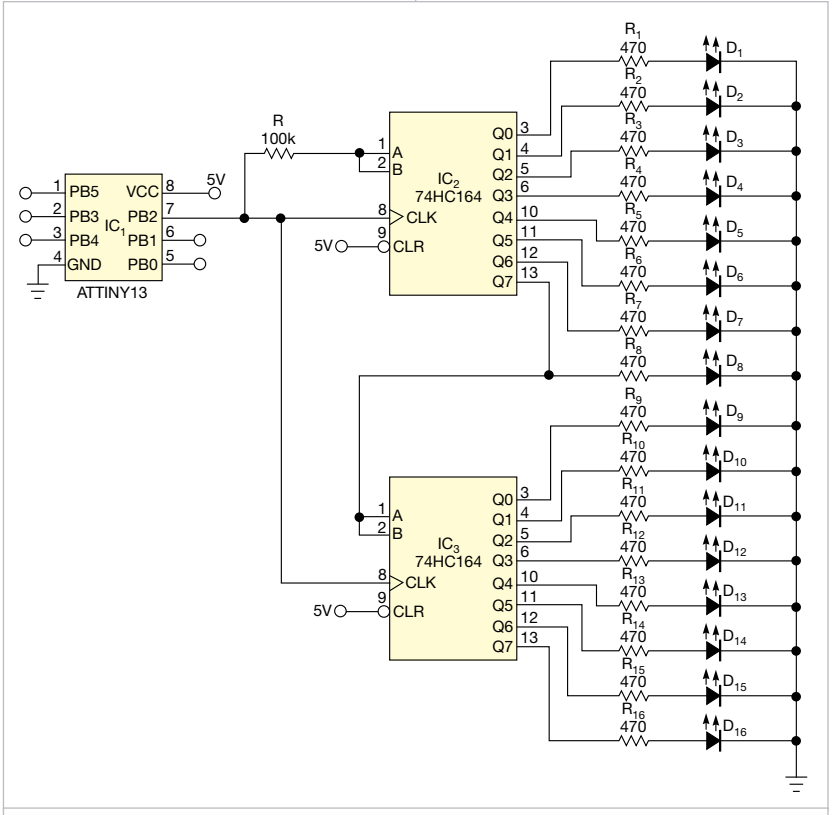

Figure 1 A 16-LED dot-bar/bar-graph display uses two 8-bit serial-input/parallel-output shift registers.

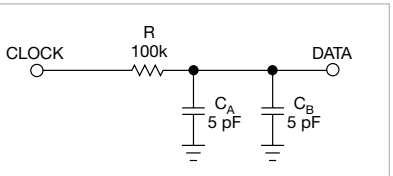

Figure 2 An RC filter provides a 0.7-µsec delay.

Figure 3 shows the clock signal in Channel 1 (yellow) and the data signal in Channel 2 (blue). The oscilloscope is a Tektronix (www.tektronix.com) DPO4034 with TPP0850 high-voltage probes. These probes have 40-MΩ input resistance and only 1.5-pF input capacitance, minimizing distortion.

A rising edge on the clock signal clocks the shift registers. This edge corresponds to the data signal's local minimum. **Figure 3** also shows that the minimum data-signal voltages for logic zero and logic one are 1.3 and 3.1V, respectively. The shift register's logical threshold is 2.5V. These voltages guarantee sufficient voltage margins. If your design requires higher margins, vary the signal timing and use a higher resistance for R in **Figure 1**. This circuit stores 16 bits in shift registers in approximately 35 µsec.

You can view a short video of the circuit in operation and download a code listing, in C, at the online version of this Design Idea at www.edn.com/110609dia. The software turns on

Get an edge: universal USB charging

Mess vs. less

As consumers buy more portable devices, they become overwhelmed with managing the various power adapters that have nonstandard connectors. To solve this problem, the micro USB connector has been universally accepted for battery charging and data transmission. Though USB requirements are complex, Maxim's charger detection, overvoltage protection, and current-limit switching ease the implementation of micro USB connectors to simplify the user experience.

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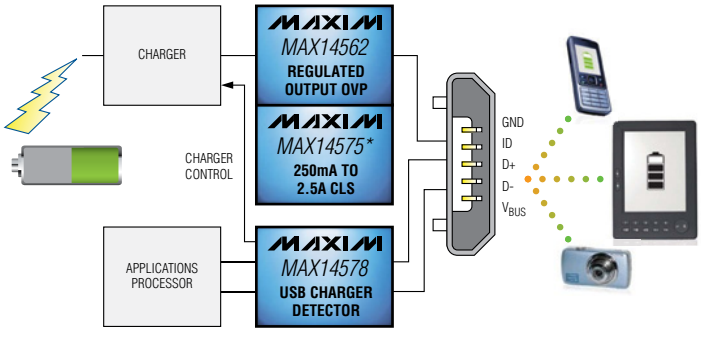

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the LEDs one by one every 500 msec until all LEDs are on. It then turns off all the LEDs and repeats the cycle. EDN

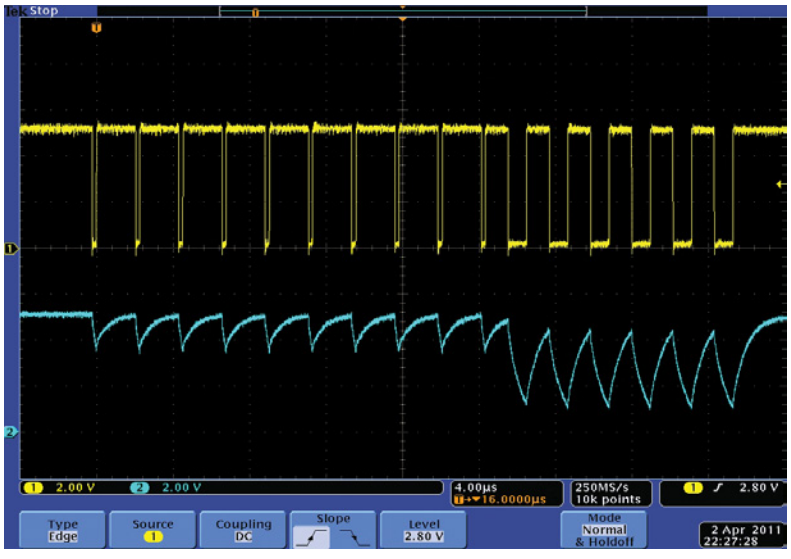

Figure 3 The waveform shows the circuit writing the pattern 1111111111000000 for the display. The upper, yellow trace is the clock signal, and the lower, blue trace is the data signal.

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Circuit measures battery capacity

Vladimir Oleynik, Moscow, Russia

Batteries and energy cells lose their capacity as they age. If a cell or battery's capacity is too low, your equipment may also soon stop working. You can use the circuit in **Figure 1** to measure a battery's discharge time. The circuit uses an electromechanical clock and a DVM (digital voltmeter). The cell should be fully charged before testing. The circuit discharges the cell at a fixed current and measures the time it takes to discharge the cell from 100 to 0%.

For example, if a manufacturer rates a cell's capacity and you discharge the cell at a constant current equal to 0.1 times the capacity, the cell should take about 10 hours to discharge from full to empty. Manufacturers of NiCd (nickel-cadmium) or NiMH (nickel-metal-hydride) cells rate the end of the discharge voltage at 1V. At that point, the cell is using 0% of its capacity, is flat, and requires charging for further operation. If this procedure takes less than 10 hours, the cell's capacity is less than what the cell manufacturer rates.

Before testing the cell, charge it to full capacity using your charger. Apply 12V dc to the circuit and use potentiometer P_2 to set a voltage of 1V at Pin 6 of IC_{1B}. Set the clock to 12:00. An AA-size, 1.5V cell powers the clock through relay switch S_3.

When you press the momentary pushbutton switch, S_1, the tested cell starts to discharge through transistor Q_1 and resistor R_1. Set the discharge current using potentiometer P_1. Op amp IC_{1A} keeps the voltage across resistor R_1 constant, thus providing stable cell-discharge current. Set the DVM to measure the dc voltage and measure the voltage across R_1. The display shows discharge current in amperes. For example, 0.25V corresponds to 0.25A. Because the initial cell voltage is higher than 1V, Pin 7 of op amp IC_{1B} is high, transistor Q_2 is on, and the DPST (double-pole/single-throw) relay coil is active. Relay-contact switch S_2 closes and bypasses the start pushbutton switch, S_1, which keeps the discharge process active. Closed relay-contact switch S_3 lets the clock keep time.

When the cell's voltage is equal to the end-of-discharge value, 1V, IC_{1B}'s output goes low and deactivates the relay coil, halting the discharge process. The clock also stops. To get the cell's capacity, multiply the set discharge-current value by the elapsed time. If the discharge-current value is small and the time necessary for the discharge of a cell is longer than 12 hours, you must check this value every 12 hours after you start the test and keep in mind laps of one to 12 hours.

This circuit also lets you estimate the self-discharge rate of the cell or battery you use. Charge your cell to 100% of its capacity and measure cell capacity

according to this procedure. Charge your cell again, store it for a month, and then measure the cell capacity again. The difference between the two values is the monthly self-discharge rate.

If you arrange the cells in a stack, you should provide a reference voltage that's higher than the battery's end-of-discharge voltage. If the battery voltage is higher than 12V, use a higher-voltage value to power the circuit. Furthermore, the reference voltage value should be higher than the battery's end-of-discharge value. Specifications of the discharge path comprising transistor Q_1 and resistor R_1 should fit higher discharge-current requirements.

The circuit works with cells or batteries of any chemistry, including NiCd, NiMH, lead acid, and lithium-ion. You can also use this circuit to measure the real capacity of nonrechargeable cells, such as AA alkaline cells. In that case, the discharged cell's voltage should be equal to the lowest power-supply voltage of your device. A cell that has passed the test is not suitable for further use, but you can use its capacity information to estimate the capacity of the batteries of the same type and manufacturer. EDN

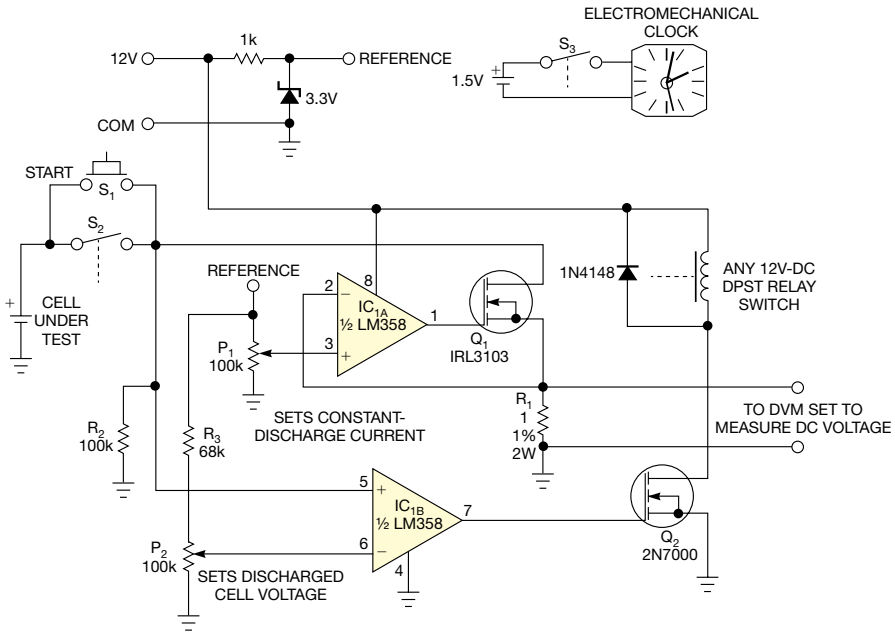

Figure 1 An electromechanical clock indicates a battery's discharge time.

Programmable driver targets piezoelectric actuators

P Saxena, VK Dubey, IJ Singh, and HS Vora, Raja Ramanna Centre for Advanced Technology, Indore, India

Motors using piezoelectric screws and linear/stack piezoelectric actuators make good choices for precise positioning (**Reference 1**). These motors typically use feedback control for applications such as optical mounts in wavelength scanning and in cavity-length stabilization. The motors are smaller than stepper motors, are lightweight and efficient, and provide fine resolution. Unfortunately, they need complex driver circuits with programmable waveshapes.

Commercially available OEM driver circuits may suffer from EMI (electromagnetic-interference)-immunity problems or can cost approximately $500. The circuit in

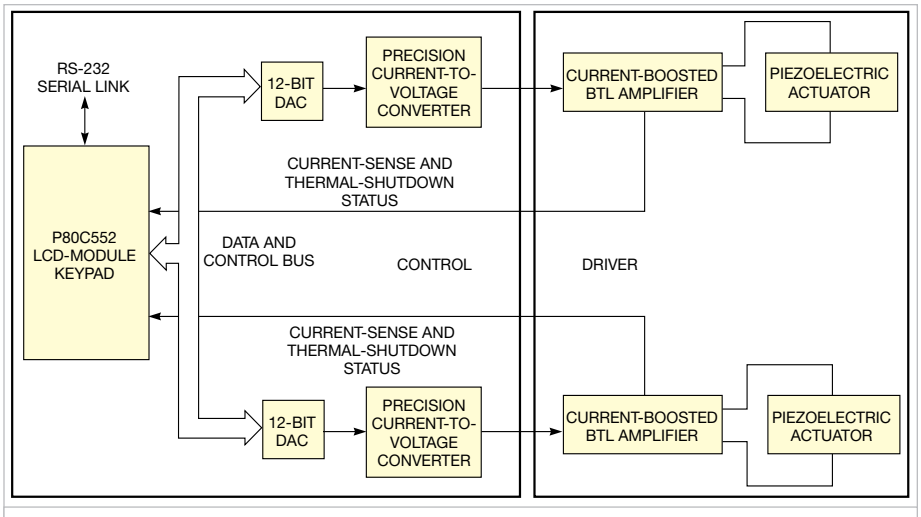

Figure 1 The controller comprises a microcontroller and a BTL-driver unit.

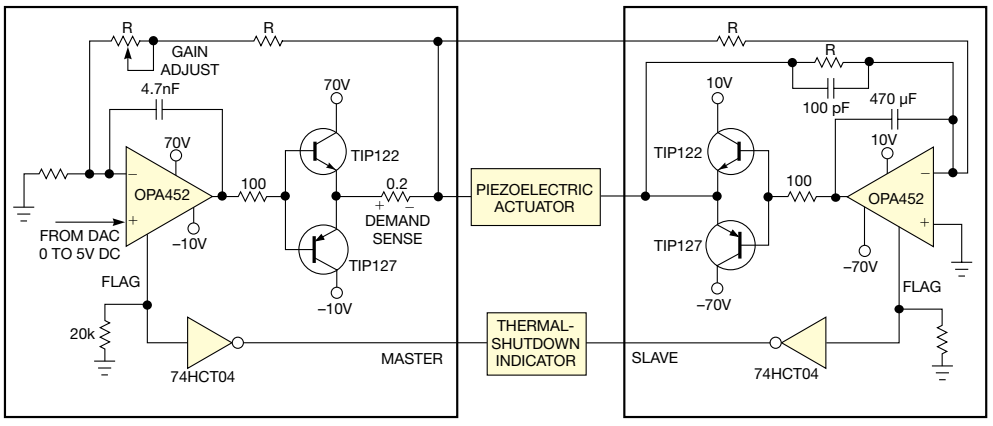

Figure 2 The circuit comprises a pair of low-cost OPA452 power op amps, which act as the BTL and drive the screw-type piezoelectric actuator.

this Design Idea presents a low-cost, microcontroller-based, multiaxis programmable driver for piezoelectric actuators.

Piezoelectric actuators often receive their power from unipolar drivers, which have slow slew rates. In this design, a microcontroller powers a universal BTL (bridge-tied-load) power amplifier. A BTL configuration doubles the slew rate, which is important in piezoelectric-drive applications. The microcontroller generates the pulse shape necessary for the forward and backward movements of actuators at a selectable speed of 0.1 Hz to 1.5 kHz. For interfacing two motors to run simultaneously, you can program synchronized speeds in an integer ratio of 1-to-N.

The circuit in **Figure 1** comprises a microcontroller and a BTL-configured driver unit. The P80C552 microcontroller uses two numbers of the 12-bit DACs, which have a conversion time of 2 µsec. These DACs directly connect to ports P3 and P4 of the microcontroller for fast response. Using this configuration, you can generate programmable waveshapes. Screw-based piezoelectric actuators need a waveshape with a rise time of approximately 110 µsec and a fall time of approximately 12 µsec to move clockwise and a mirror of it for counterclockwise motion. Software in 8051 assembly language can generate the waveforms for these motions. Using slow ramps, the system can control a linear piezoelectric actuator.

You can use the front-panel LCD and keypad to select the operations for setting the speeds, the motors, and the direction, or you can remotely set them using an RS-232 interface. You must make sure that on/off transients don't cause motor motion.

The heart of the design is a precision power driver. You can model the device using one capacitor with an impedance of $1/\omega C$. Current rises with frequency when a periodic voltage source has a frequency lower than the actuator's resonant frequency. The BTL is an output configuration for power amplifiers in which the load—the actuator—connects between two amplifiers, bridging the output terminals. This action makes the voltage swing at the load twice that of single-ended amplifiers with the outputs driven in opposite phases.

Figure 2 shows a pair of low-cost OPA452 power op amps, which act as the BTL and drive the screw-type piezoelectric actuator, which receives its asymmetric power supplies at ±70 and ±10V. This configuration delivers an output swing of 140V with a slew rate that is twice that of a unipolar device. Internal diodes comprising Darlington transistors offer flyback protection. Connecting the ultrafast diodes from the output to their corresponding power-supply rails can also protect each amplifier. To enhance the output current at as much as 1A, use external transistors in complementary symmetry mode.

WHEN OPERATING IN STATIC MODE, THE CIRCUIT IN ITS DRIVING VOLTAGE HAS A RIPPLE OF LESS THAN 20 mV. IT ACHIEVES FULL-SCALE OUTPUT-VOLTAGE POSITIONAL ACCURACY.

The circuit in **Figure 2** is valid for both static and ac operation. Static operation requires low current, and, for ac operation, the current is proportional to the rate of change of the driving voltage. In this case, the driver can supply a peak current of as much as 1A. When operating in static mode, the circuit in its driving voltage has a ripple of less than 20 mV. It achieves good full-scale output-voltage positional accuracy. A 100Ω resistance limits the current through the OPA452.

The system's full-power bandwidth is 3.5 kHz, and it provides thermal-shutdown and current-limiting features.

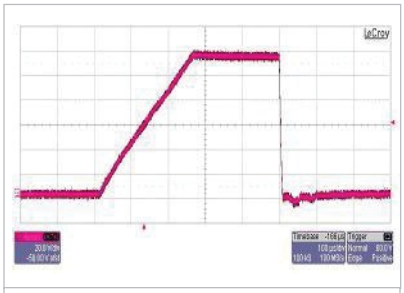

Figure 3 An oscilloscope shows the driver circuit's slow rise time and fast fall time.

Figure 3 shows the driver output of the system as tested with a piezoelectric screw. This pulse shape with slow rise time and fast fall time moves the piezoelectric screw clockwise. It has a differential output of 122V with a proportional gain of 24. Testing the driver with picomotors and linear actuators shows a step size of 30 nm/pulse and linear movement of 50 nm/V, respectively.

The drive can synchronize the etalon, and the tuning mirror handles hop-free tuning of a narrow-bandwidth dye laser. In a single-axial-mode dye-laser setup, the circuit can obtain approximately 25-GHz hop-free mode tuning by synchronizing the movement of the tuning mirror angle and etalon tilt. EDN

REFERENCE

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Circuit boosts voltage to piezoelectric transducers

Kurt Nell, Sankt Pölten, Austria

Piezoelectric transducers are common in ultrasonic and acoustic-alarm-signaling applications. To get enough acoustic power from a piezoelectric transducer, you must power the device with a frequency at or near its resonant frequency. Furthermore, the driving voltage should be as high as the transducer allows.

A transformer circuit drives the transformer and the transducer at resonant frequency. You must usually build and optimize these transformers for the transducer you are using—a time-consuming job. You can, however, drive the piezoelectric transducer without the transformer using the circuit in **Figure 1**.

The circuit includes an oscillator using Schmitt trigger IC_{1A}. The frequency depends on resistor R_1 and capacitor C_1. You must select both components to fit the oscillator frequency with the resonant frequency of the piezoelectric transducer. You can replace R_1 with a variable resistor and change the value to maximize the voltage on the transducer.

The driver includes the five additional inverters of IC_1, IC_{1B} through IC_{1F}. A voltage tripler comprises diodes D_1 and D_2 and the surrounding components. The amplifier comprises Q_2, and the piezoelectric driver comprises Q_1 and Q_2.

Diodes D_1 and D_2 come in one BAS40-04 package. Alternatively, you can use double transistors for Q_1, Q_2, and Q_3. You can replace the oscillator with a microcontroller if you have one available. The circuit works with supply voltages of less than 10V. You can use it in 3.3V systems, but you should then use a 74HC14 inverter for the oscillator and the driver. You can also use additional voltage-doubler stages to get even more driving voltage for the transducer. EDN

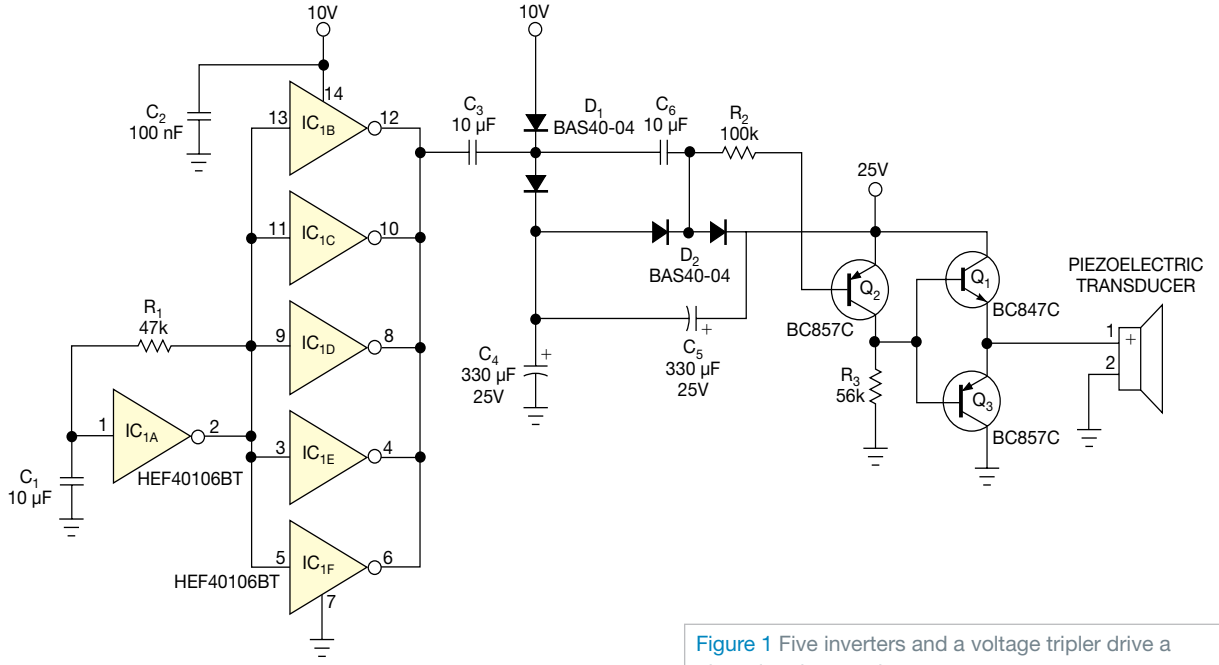

Figure 1 Five inverters and a voltage tripler drive a piezoelectric transducer.

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LINKING DESIGN AND RESOURCES

Light, life, and LEDs: taking LEDs beyond lighting

The future for LEDs is a bright one, but not only in lighting. When you properly apply these components, they can provide additional benefits beyond lighting up a room, including health advantages, according to Cary Eskow (**photo**), global director of lighting-business development at Avnet Electronics Marketing (www.em.avnet.com).

Back by popular demand, Eskow returned to be the keynote speaker at *EDN*'s "Designing with LEDs" seminar and hands-on workshop, which took place last month in San Jose, CA. His presentation, "Light, Life, and LEDs," acknowledged the tremendous impact of high-brightness LEDs as clean, safe, and energy-efficient sources of light. However, throughout the keynote address, Eskow pointed to a multitude of new applications that this technology may enable, well beyond basic interior and exterior lighting.

"If I were to ask you what the most significant benefit of LEDs are, what would you say?" he asked. "I imagine most people would say energy conservation—maybe total cost of ownership. All of these [benefits] are great advantages, but here we are, almost halfway through 2011, and how many LED lights do you see in this room? Not one."

Eskow gave two possible reasons for the absence of advanced lighting in the large hotel conference room. "There are some challenges in developing the system-level knowledge of a high-brightness application—thermal issues, dimming, all those things." This area represents a design-chain opportunity for distributors within the electronics supply chain, including Avnet, that have stepped in to help engineers and lighting professionals iron out questions in this relatively new design category.

"But I believe the fundamental reason [for the absence of advanced lighting in the room] is that the value proposition is not compelling enough," Eskow continued. "Why would someone go out and spend more money for a product that does what an existing product does? Mathematically, it's undeniable that there are savings and other benefits, but proof positive is what we see in this room."

Eskow has worked closely with OEMs (original-equipment manufacturers), LED manufacturers, advanced-analog-IC vendors, and secondary-optics vendors since he received his first patent using LEDs two decades ago. He noted that the people who traditionally make luminaires are craftsmen who may be unaware of what they can do with an LED. "They may not be aware of the physiological impacts of doing things with an LED or light in general—that can change it from just a light source to a health benefit."

Controlling light through such

techniques as dimming and pulse modulation will advance this process. Yet Eskow pointed out that luminaire craftsmen can do only what they know is possible.

He used Jules Verne's *From the Earth to the Moon* to illuminate his point. The characters in Verne's book applied a cannon as a means of launching themselves to the moon. This form of transportation and force was the fastest available in 1865 when the book was published. "Just as Jules Verne may not have been aware of what would be possible [now], these luminaire craftsmen may be unaware of the future possibilities of LEDs and other forms of lighting," Eskow said.

Controlling light temperatures offers not only revenue benefits but also physiological benefits, such as enhanced concentration, more desirable perceptions of food or a room, and medical advantages. "By adding a few dollars' worth of components to a sconce on a wall, you can sell it at basic market price and then contact the user and say, 'If you are interested, I'll tell you how to enable this digital feature for a fee.' This [approach]," Eskow explained, "allows for a revenue stream that not only incorporates the source but also has the [continued benefit] that the customer could sometime later provide more revenue."

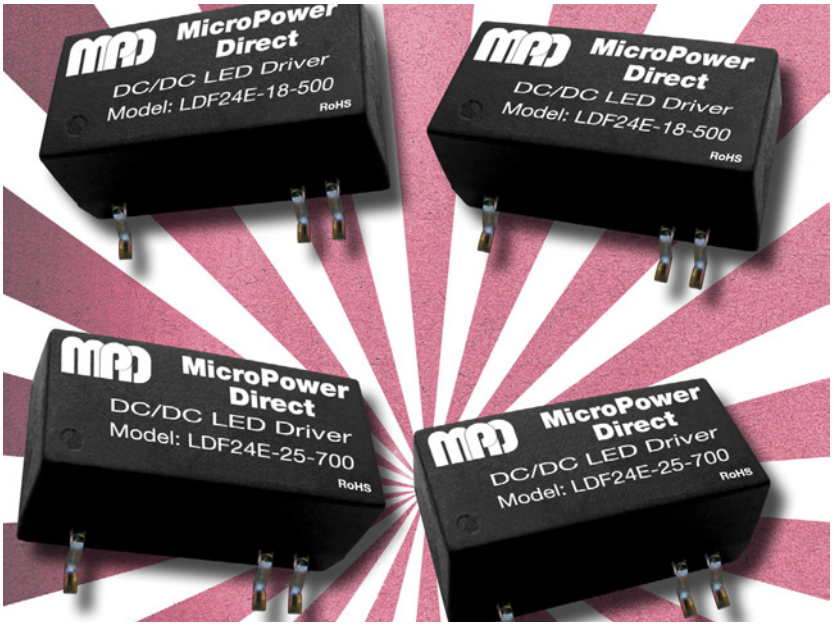
The physiological and health benefits include the use of light for Vitamin D synthesis, enhanced attentiveness in humans, and light-induced polyphenol production in plants. Eskow specifically noted the blue- and ultraviolet-light ranges, pointing out that, if we don't properly use these ranges, the effects can be dangerous or harmful. For example, light influences melatonin, a naturally occurring compound in animals, plants, and microbes, and affects many things, including sleep and wake cycles.

"Melatonin appears to have anticarcinogenic qualities, such as by changing the molecular-adhesion characteristics of blood cells," Eskow said. "Recent published research suggests a link between workers, such as night-shift nurses exposed to a lot of cool-blue light, and elevated cancer risks. These things can really change the game for solid-state lighting; a little bit of blue, knowledgeably and carefully put in there, can make it more than just a light source."

Eskow noted that we are at just the beginning of realizing these benefits. Just as Verne was unaware of potential new propulsion technologies, the future is full of possibilities for new lighting applications that we cannot yet conceive of.

productroundup

POWER SOURCES



Constant-current LED drivers control high-brightness LEDs

The LDF24E series of dc/dc drivers powers and controls high-brightness LEDs. The units feature constant-current outputs of 300, 350, 500, 600, or 700 mA. Their step-down dc/dc design allows them to drive strings with voltage as high as 36V dc. They provide efficiency as high as 96%, short-circuit protection, and separate analog- and PWM-dimming-control inputs. MTBF is greater than 2 million hours. The devices come in miniature SMT packages. The 300- and 350-mA models operate over the industrial-temperature range of –40 to +85°C ambient with no derating or heat-sinking. Other models operate at temperatures as high as 71°C. Free-air convection provides cooling. Prices for the 300-, 350-, 500-, 600-, and 700-mA devices are $5.75, $6.45, $6.80, $7.15, and $7.90, respectively.
MicroPower Direct, **www.micropowerdirect.com**

Zero-power ac/dc PWM controller enables offline adapters and chargers

The iW1700 zero-power ac/dc digital PWM controller enables low-cost, energy-efficient 120/230V-ac offline adapters and chargers requiring as much as 5W, which consume zero no-load power for cell phones; audio players; digital cameras; and other low-power, portable devices. The device uses patented adaptive digital PWM/PFM technology that sends the controller into sleep mode when you disconnect the load, cutting no-load power consumption to less than 4 mW—effectively zero because the IEC 62301 standard for measuring standby power in household electrical appliances rounds power usage of 5 mW or less to zero. Digital techniques enable the iW1700 to support primary-side control, eliminating the need for an optocoupler. It also features quasiresonant switching for low EMI, cycle-by-cycle waveform analysis, and a switching frequency as high as 72 kHz to achieve no-load charger performance, meet manufacturers' power-supply requirements, and still enable a low BOM cost. The iW1700 comes in a low-cost, standard six-pin SOT-23 package and sells for 25 cents (10,000).

iWatt, **www.iwatt.com**

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stant-power regulation from 8 or 14V-dc primary outputs and can drive highly capacitive loads, including supercapacitors, as well as relays, solenoids, SSRs, indicating lights, op-amp drivers, zero-crossing detectors, and RF/power-line-carrier transceivers. Dual-output versions are also available with a secondary dc output of 3.3 or 5V dc. During standby operation, no-load power consumption is 30 mW or less. Prices start at $7 (OEM quantities).

Bias Power, www.biaspower.com

Power-supply ICs target AMOLED displays

The single-chip STOD03A AMOLED (active-matrix-organic-LED) power-supply ICs provide positive and negative supply voltages from a single chip. Completing the power-supply circuitry requires only six external components. The STOD03A features a 4.6V fixed positive output voltage, a programmable negative output voltage of −2.4 to −5.4V, and a 200-mA output current. The device's 1.5-MHz operation allows the use of small external components, lets the enable pin control shutdown mode, and provides accurate output voltages with low cellular noise. The device is in full production, comes in a 3×3×0.6-mm, 12-lead DFN12L package, and sells for 80 cents (1000).

STMicroelectronics, www.st.com

Switching power supplies target use in industrial electrical-control panels

This series of DIN-rail-mounted, single- and three-phase switching power supplies targets use in electrical-control panels and features 20 to 960W wattages. The power-supply outputs are 5, 12, or 24V dc and have short-circuit and overload protection. A digital status display shows the output voltage, output current, peak current, temperature, and running hours. The UL- and CE-approved supplies come with a two-year warranty, and prices start at $25.

Electrotech Direct, www.esgllc-usa.com

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Hammer it home

Several years ago, I worked for a company that makes expensive fiber-optic transceivers. The company worked with a vendor that made burn-in racks for hundreds of the laser diodes that these transceivers used. It was my job to check out and debug any problems in the design. The racks had hundreds of relays that would switch the system's voltmeter to appropriate nodes to measure the voltage and current of any given laser. Just by looking at the schematic, I saw a problem. The rack vendor had no series resistors in the relay connections to the voltmeter. If a bad software command simultaneously energized two relays, they would tie parts of the circuitry together that were not intended to connect and perhaps even blow the lasers.

I believe I mentioned that they were expensive lasers. So I asked the company to add the series resistors, which they begrudgingly did.

Because these lasers were new, initial volume did not allow me to fully load the racks. Small batches ran fine. However, as production ramped up and I finally loaded the racks with lasers, trouble started. As the racks cycled through their voltmeter measurements, bad voltmeter readings would intermittently occur. Often, every reading after the initial bad reading would also be bad.

The vendor's software would interpret bad readings as a bad laser. The software would then turn off the bad lasers and mark them as bad in the database, so they never experienced the full burn-in. This problem threatened my company's production goals. As it turned out, relays that should not have been operating occasionally remained on when they were in the rack.

Oddly, this situation was not the result of some software glitch. I gained access to some of the relay coils with a DVM (digital voltmeter) and figured out that the relay was going in at the proper time but was not releasing, even though the coil was no longer energized.

When I looked at the routing of the power and ground to these high-power lasers, I understood. The rack vendor had simplified the routing by separating the high-current power and ground cables to different sides of the rack. Worse yet, the power cables looped up and around the relays. That big loop of high current created a magnetic field—too weak to pull in any of the relays but enough to keep a relay or two in even when the test program had turned off the coil current.

The technician I was working with was skeptical that the field with only one loop could hold in a relay. During the next malfunction, I carefully placed a large ball-peen hammer near the card cage with the relays. The hammer head coaxed enough flux from the offending relay, and good voltmeter readings resumed. The technician was now a believer.

We routed the power and ground cables as close together as we could, but there was no easy way to remove the big loop of power cables that circled the relays. So we fashioned a ¼-in.-thick steel plate to shield the relays, solving the problem. Nevertheless, the test group still had to flip the plate over every six months or so because it was becoming magnetized and not working as well as I had intended.

It was a good thing that the vendor added the series resistors because these shorting events were sure to have blown out some of the lasers—something your burn-in rack should avoid doing. EDN

Roy Timpe is a senior engineer with 27 years of experience in measurement development and automation.

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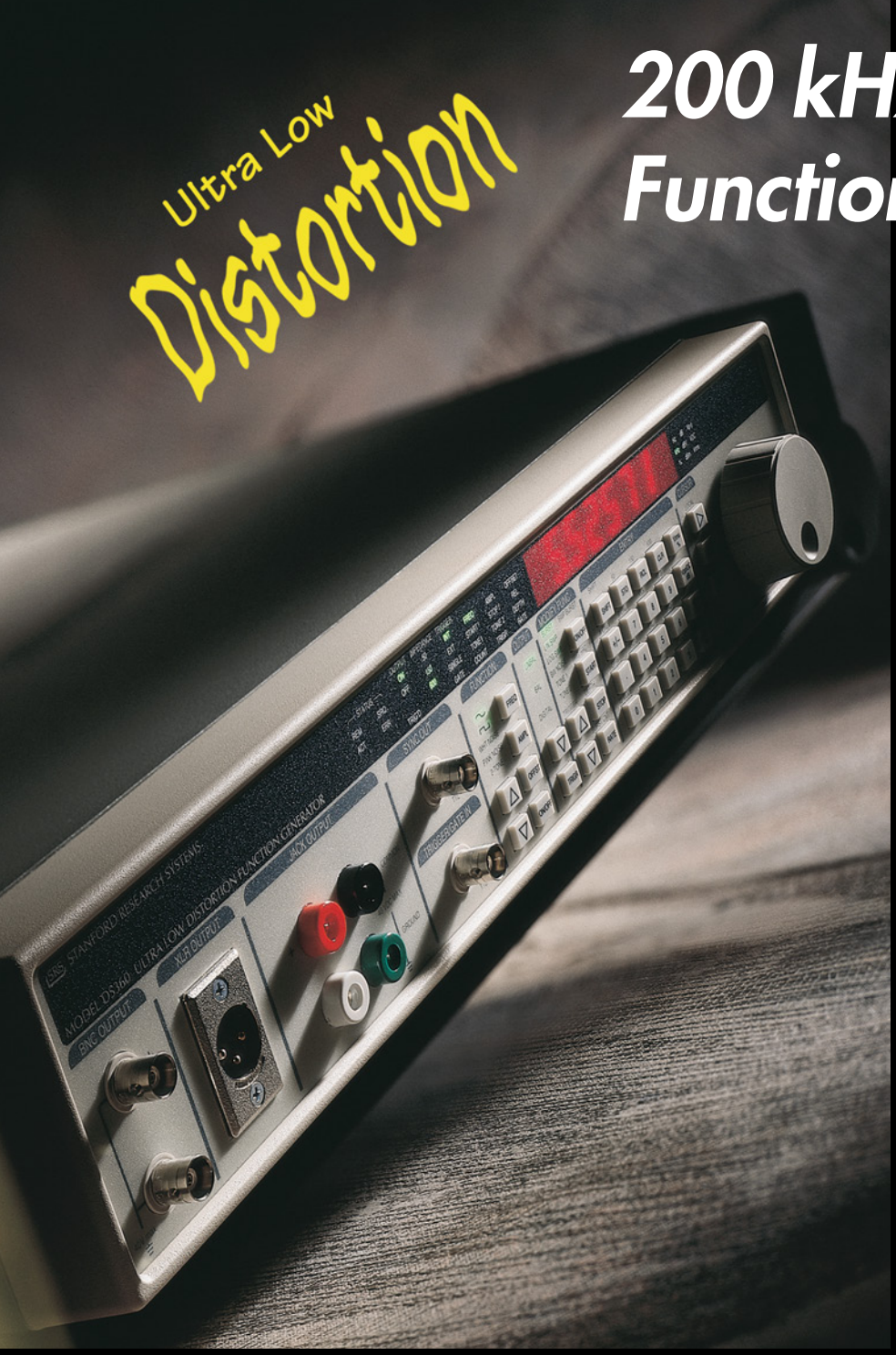

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